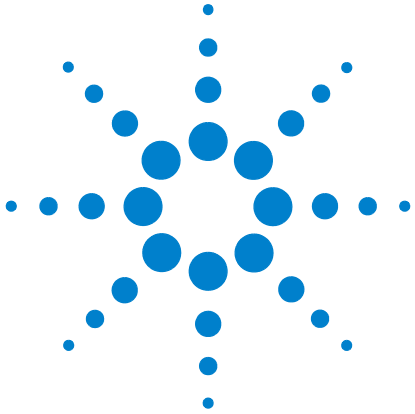

# Agilent U7233A DDR1 Compliance Test Application

## Compliance Testing Notes

Agilent Technologies

# Notices



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# Quick Reference

**Table 1** Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

| TEST | Cycle | | Based on Test Definition | | | | | | Required to Perform on Scope | | | | | | Opt. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Read | Write | DQ | DQS | CK | ADD | Ctrl | Data Mask Ctrl | DQ | DQS | CK | ADD | Ctrl | Data Mask Ctrl | CS# |
| SlewR | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| SlewF | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| VIH(ac) | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| VIH(dc) | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| VIL(ac) | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| VIL(dc) | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| VOH(ac) | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| VOL(ac) | | √ | √ | √ | √ | √ | √ | | √[2] | √[2] | √[2] | √[2] | √[2] | | |
| AC Overshoot | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| AC Undershoot | | √ | √ | √ | √ | √ | √ | √ | √[2] | √[2] | √[2] | √[2] | √[2] | √[2] | |
| VID(ac) | | √ | | √ | √ | | | | | √[3] | √[3] | | | | |
| VIX(ac) | | √ | | √ | √ | | | | | √[3] | √[3] | | | | |
| tAC | √ | | √ | | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tDQSCK | √ | | | √ | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tCK(avg) | | | | | √ | | | | | | √[2] | | | | |
| tCH(avg) | | | | | √ | | | | | | √[2] | | | | |
| tCL(avg) | | | | | √ | | | | | | √[2] | | | | |
| tHZ(DQ) | √ | | √ | | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tHZ(DQS) | √ | | | √ | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tLZ(DQS) | √ | | | √ | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tLZ(DQ) | √ | | √ | | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tDQSQ | √ | | √ | √ | | | | | √[2] | √[2] | √[2] | | | | √ |
| tQH | √ | | √ | √ | | | | | √[2] | √[2] | √[2] | | | | √ |

**Table 1** Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

| TEST | Cycle | | Based on Test Definition | | | | | | Required to Perform on Scope | | | | | | Opt. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Read | Write | DQ | DQS | CK | ADD | Ctrl | Data Mask Ctrl | DQ | DQS | CK | ADD | Ctrl | Data Mask Ctrl | CS# |
| tDQSS | | √ | | √ | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tDQSH | √ | | | √ | | | | | √[2] | √[2] | √[2] | | | | √ |
| tDQSL | √ | | | √ | | | | | √[2] | √[2] | √[2] | | | | √ |
| tDSS | | √ | | √ | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tDSH | | √ | | √ | √ | | | | √[2] | √[2] | √[2] | | | | √ |
| tWPST | | √ | | √ | | | | | √[2] | √[2] | √[2] | | | | √ |
| tWPRE | | √ | | √ | | | | | √[2] | √[2] | √[2] | | | | √ |
| tRPRE | √ | | | √ | | | | | √[2] | √[2] | √[2] | | | | √ |
| tRPST | √ | | | √ | | | | | √[2] | √[2] | √[2] | | | | √ |
| tDS(base) | | √ | √ | | | | | | √[2] | √[2] | √[2] | | | | √ |
| tDH(base) | | √ | √ | | | | | | √[2] | √[2] | √[2] | | | | √ |
| tIS(base) | √ | | | | √ | √ | √ | | | | √[2] | √[2] | √[2] | | √ |
| tIH(base) | √ | | | | √ | √ | √ | | | | √[2] | √[2] | √[2] | | √ |
| High State Ringing | | | √ | √ | | √ | √ | √ | √[1,2] | √[1,2] | | √[1,2] | √[1,2] | √[1,2] | |
| Low State Ringing | | | √ | √ | | √ | √ | √ | √[1,2] | √[1,2] | | √[1,2] | √[1,2] | √[1,2] | |
| tJIT(per) | | | | | √ | | | | | | √[2] | | | | |
| tJIT(cc) | | | | | √ | | | | | | √[2] | | | | |
| tERR(nper) | | | | | √ | | | | | | √[2] | | | | |
| tJIT(duty) | | | | | √ | | | | | | √[2] | | | | |

## DDR1 Compliance Test Application — At A Glance

The Agilent U7233A DDR1 Compliance Test Application is a DDR (Double Data Rate) test solution that covers electrical, clock and timing parameters of the JEDEC (Joint Electronic Device Engineering Council) specifications, specifically *JESD79E*. The software helps you in testing all the un-buffered device under test (DUT) compliance, with the Agilent 54850A, 8000 and 80000 series Infiniium digital storage oscilloscope.

There are 2 main categories of test modes:

- Compliance Tests - These tests are based on the DDR JEDEC compliance specifications and are compared to corresponding compliance test limits.
- Debug Mode - These tests are not based on any compliance specification. The primary use of these tests is to perform signal debugging.

The DDR1 Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

The minimum number of probes required for the tests are:

- Clock tests - 1 probe.
- Electrical tests - 3 probes.
- Clock Timing tests - 3 probes.
- Advanced Debug tests - 3 probes.

**NOTE** The tests performed by the DDR1 Compliance Test Application are intended to provide a quick check of the physical layer performance of the DUT. These tests are not replacement for an exhaustive test validation plan.

DDR SDRAM electrical, clock and timing test standards and specifications are described in the *JESD79E* document. For more information, please refer to JEDEC web site at www.jedec.org.

## Required Equipment and Software

In order to run the DDR1 automated tests, you need the following equipment and software:

- 54850A, 8000 or 80000 series Infiniium Digital Storage Oscilloscope. Agilent recommends using 4 GHz and higher bandwidth oscilloscope.
- Infiniium software revision 05.30 or later.
- U7233A DDR1 Compliance Test Application, version 1.0 and higher.
- RAM reliability test software.
- 1169A, 1168A, 1134A, 1132A or 1131A InfiniiMax probe amplifiers.
- N5381A or E2677A differential solder-in probe head, N5382A or E2675A differential browser probe head, N5425A ZIF probe head or N5426A ZIF tips.
- Any computer motherboard system that supports memory.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

Below are the required licenses:

- U7233A DDR1 Compliance Test Application license.
- N5414A InfiniiScan software license (for 80000 and 54850A series).
- N5415A InfiniiScan software license (for 8000 series).
- N5404A Deep memory option (optional).

## In This Book

This manual describes the tests that are performed by the DDR1 Compliance Test Application in more detail; it contains information from (and refers to) the *JESD79E*, and it describes how the tests are performed.

- Chapter 1, “Installing the DDR1 Compliance Test Application” shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the DDR1 Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “Single-Ended Signals AC Input Parameters Tests” shows how to run the single-ended signals AC input parameters tests. This chapter includes maximum ac output logic high and minimum ac output logic low.
- Chapter 4, “Single-Ended Signals AC Output Parameters Tests” shows how to run the single-ended signals AC output parameters tests. This chapter includes input logic high tests, input logic low tests, and maximum and minimum ac output logic high and low.
- Chapter 5, “Single-Ended Signals Overshoot/Undershoot Tests” describes the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 6, “Differential Signals AC Input Parameters Tests” describes the $V_{ID}$ AC differential input voltage tests and $V_{IX}$ AC differential cross point voltage tests.
- Chapter 7, “Clock Timing (CT) Tests” describes the clock timing operating conditions of SDRAM as defined in the specification.
- Chapter 8, “Data Strobe Timing (DST) Tests” describes various data strobe timing tests including tHZ(DQ), tHZ(DQS), tLZ(DQS), tLZ(DQ), tDQSQ, tQH, tDQSS, tDQSH, tDQSL, tDSS, tDSH, tWPST, tWPRE, tRPRE and tRPST tests.
- Chapter 9, “Data Mask Timing (DMT) Tests” describes the DQ and DM input setup time and input hold time.
- Chapter 10, “Command and Address Timing (CAT) Tests” describes the address and control input setup time and input hold time.
- Chapter 11, “Advanced Debug Mode Clock Tests” describes the measurement clock tests including clock period jitter, cycle to cycle period jitter, cumulative error, and half period jitter.
- Chapter 12, “Advanced Debug Mode High-Low State Ringing Tests” shows the high state and low state ringing test method of implementation.
- Chapter 13, “Calibrating the Infiniium Oscilloscope and Probe” describes how to calibrate the oscilloscope in preparation for running the automated tests.

- Chapter 14, “InfiniiMax Probing” describes the probe amplifier and probe head recommendations for testing.
- Chapter 15, “Common Error Messages” describes the error dialog boxes that can appear and how to remedy the problem.

### See Also

- The DDR1 Compliance Test Application’s online help, which describes:
  - Starting the DDR1 compliance test application.
  - Creating or opening a test project.
  - Setting up DDR1 test environment.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running tests.
  - Viewing test results.
  - Viewing/printing the HTML test report.
  - Understanding the HTML report.
  - Saving test projects.

## Contact Agilent

For more information on DDR1 Compliance Test Application or other Agilent Technologies' products, applications and services, please contact your local Agilent office. The complete list is available at:

**www.agilent.com/find/contactus**

### Phone or Fax

**United States:**

(tel) 800 829 4444

(fax) 800 829 4433

**Canada:**

(tel) 877 894 4414

(fax) 800 746 4866

**China:**

(tel) 800 810 0189

(fax) 800 820 2816

**Europe:**

(tel) 31 20 547 2111

**Japan:**

(tel) (81) 426 56 7832

(fax) (81) 426 56 7840

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E-mail: tm_ap@agilent.com

# Contents

## 7 Clock Timing (CT) Tests



## 8 Data Strobe Timing (DST) Tests

# 1 Installing the DDR1 Compliance Test Application



If you purchased the U7233A DDR1 Compliance Test Application separately, you need to install the software and license key.

## Installing the Software

1 Make sure you have version 05.30 or higher of the Infiniium oscilloscope software by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the DDR1 Compliance Test Application, go to Agilent website: http://www.agilent.com/find/U7233A.

3 The link for DDR1 Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

## Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

# 2 Preparing to Take Measurements



Before running the DDR1 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR1 Compliance Test Application and perform the measurements.

## Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 13, "Calibrating the Infiniium Oscilloscope and Probe".

**NOTE** If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

**NOTE** If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

## Starting the DDR1 Compliance Test Application

1 Ensure that the RAM reliability test software is running in the computer system where the Device Under Test (DUT) is attached. This software performs tests to all unused RAM in the system by producing a repetitive burst of read-write data signals to the DDR memory.

2 To start the DDR1 Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>DDR1 Test**.

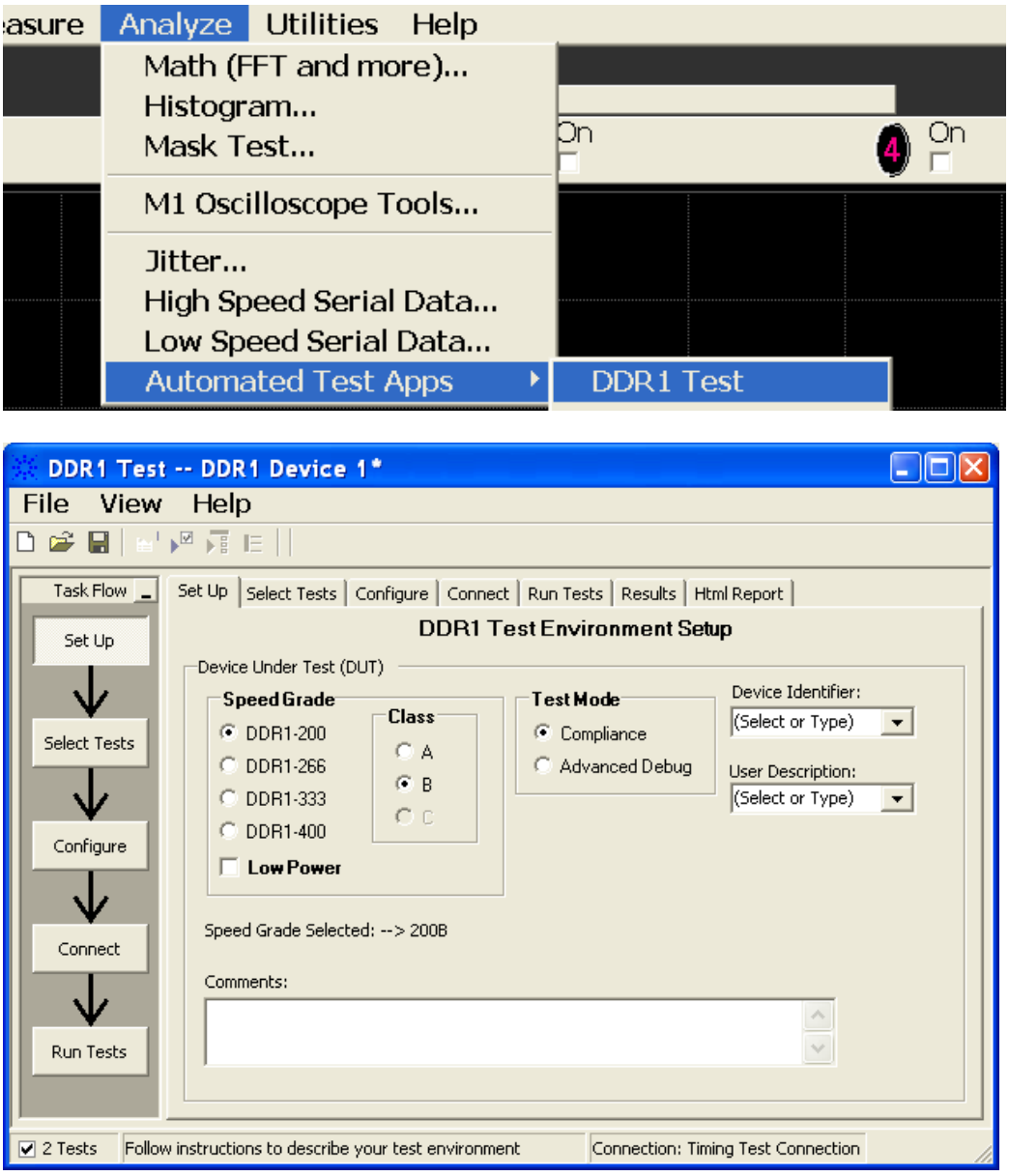


**Figure 1** The DDR1 Compliance Test Application

**NOTE** If DDR1 Test does not appear in the Automated Test Apps menu, the DDR1 Compliance Test Application has not been installed (see Chapter 1, "Installing the DDR1 Compliance Test Application").

Figure 1 shows the DDR1 Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

| | |
|---|---|
| Set Up | Lets you identify and setup the test environment, including information about the device under test. |
| Select Tests | Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups. |
| Configure | Lets you configure test parameters (like memory depth). This information appears in the HTML report. |
| Connect | Shows you how to connect the oscilloscope to the device under test for the tests to be run. |
| Run Tests | Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing. |
| Results | Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear. |
| HTML Report | Shows a compliance test report that can be printed. |

**NOTE** When you close the DDR1 application, each channel's probe is configured as single-ended or differential depending on the last DDR1 test that was run.

## Online Help Topics

For information on using the DDR1 Compliance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The DDR1 Compliance Test Application's online help describes:

- Starting the DDR1 Automated Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up DDR1 test environment.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
- Viewing test results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
- Viewing/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.

# 3 Single-Ended Signals AC Input Parameters Tests



This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Input tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

# Probing for Single-Ended Signals AC Input Parameters Tests

When performing the Single-Ended Signals AC Input Parameters tests, the DDR1 Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR1 Compliance Test Application for the exact number of probe connections.

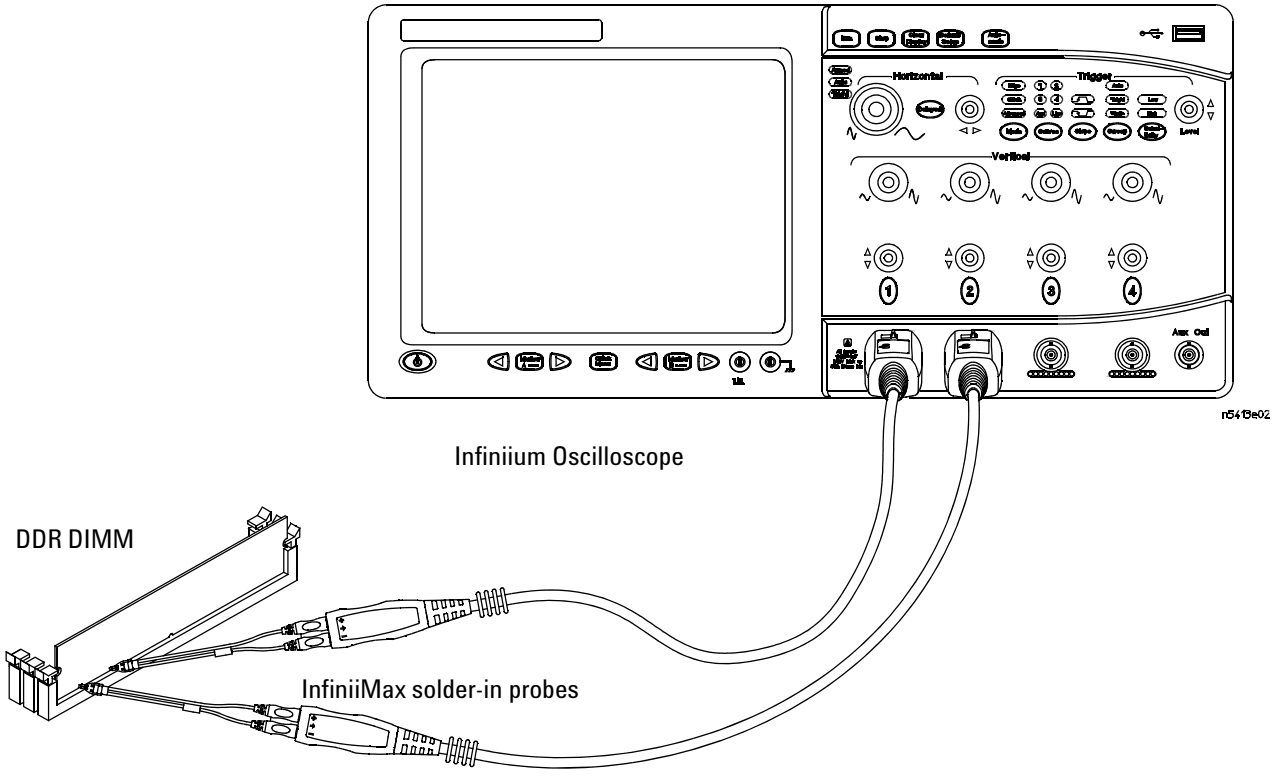


**Figure 2** Probing for Single-Ended Signals AC Input Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channels shown in Figure 2 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1. Start the automated test application as described in “Starting the DDR1 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR1 Test Application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR1-200, DDR1-266, DDR1-333, DDR1-400.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

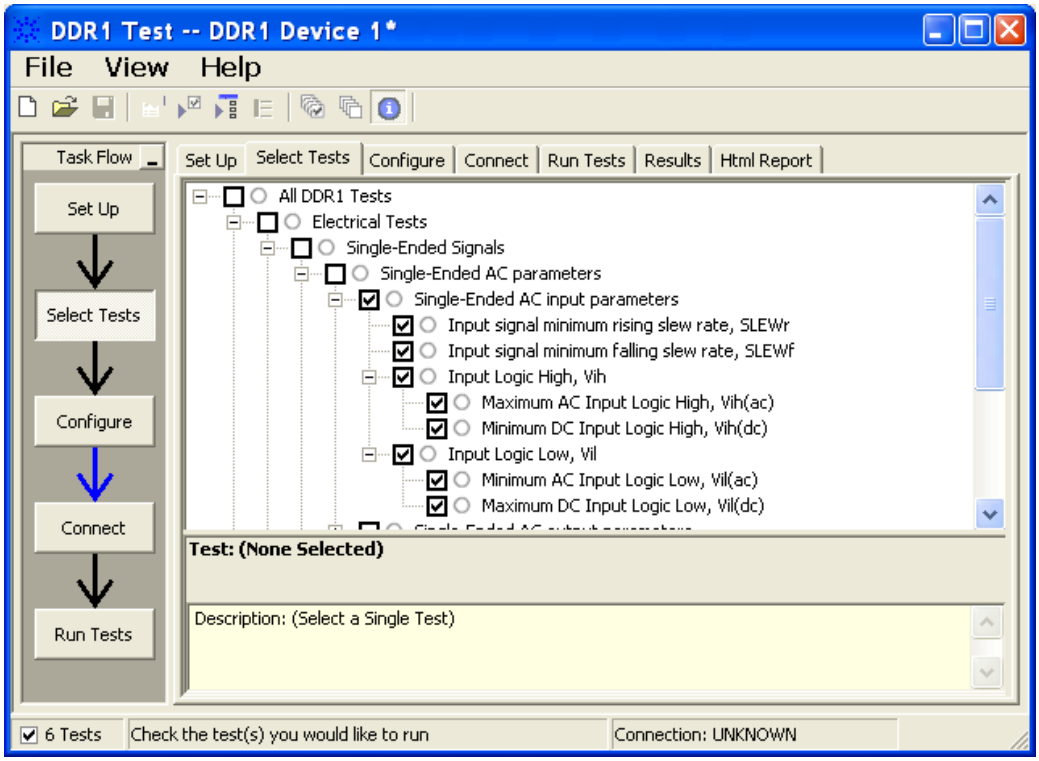


**Figure 3** Selecting Single-Ended Signals AC Input Parameters Tests

**9** Follow the DDR1 Test Application's task flow to set up the configuration options (see Table 2), run the tests and view the tests results.

**Table 2** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **InfiniiScan Limits** | |
| **Read Cycle** | |
| IScan_UL_READ | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle) |
| IScan_LL_READ | Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle) |
| **Write Cycle** | |
| IScan_UL_WRITE | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle) |
| IScan_LL_WRITE | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle) |
| **Single-Ended Signals** | |
| **Single-Ended AC Parameters** | |
| Pin Under Test, PUT | Identifies the Pin Under Test for Single-Ended AC parameters. |
| PUT Source | Identifies the source of the PUT to be analyzed for Single-Ended AC tests. |
| Supporting Pin | Identifies the required supporting pin for Single-Ended AC parameters. |
| Supporting Pin Source | Identifies the source of the supporting pin for Single-Ended AC Tests. |

# $Slew_R$ Test Method of Implementation

$Slew_R$ - Input Signal Minimum Slew Rate (Rising). The purpose of this test is to verify that the rising slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the *JEDEC Standard JESD79E*.

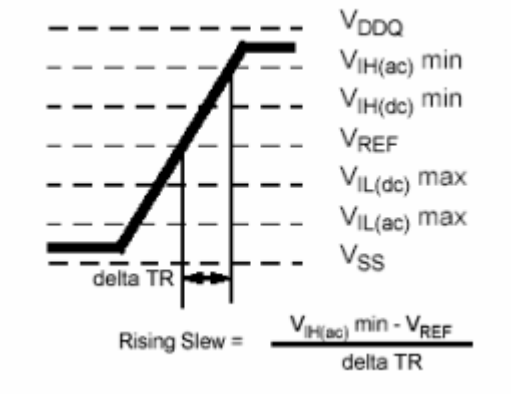


**Figure 4** $Slew_R$

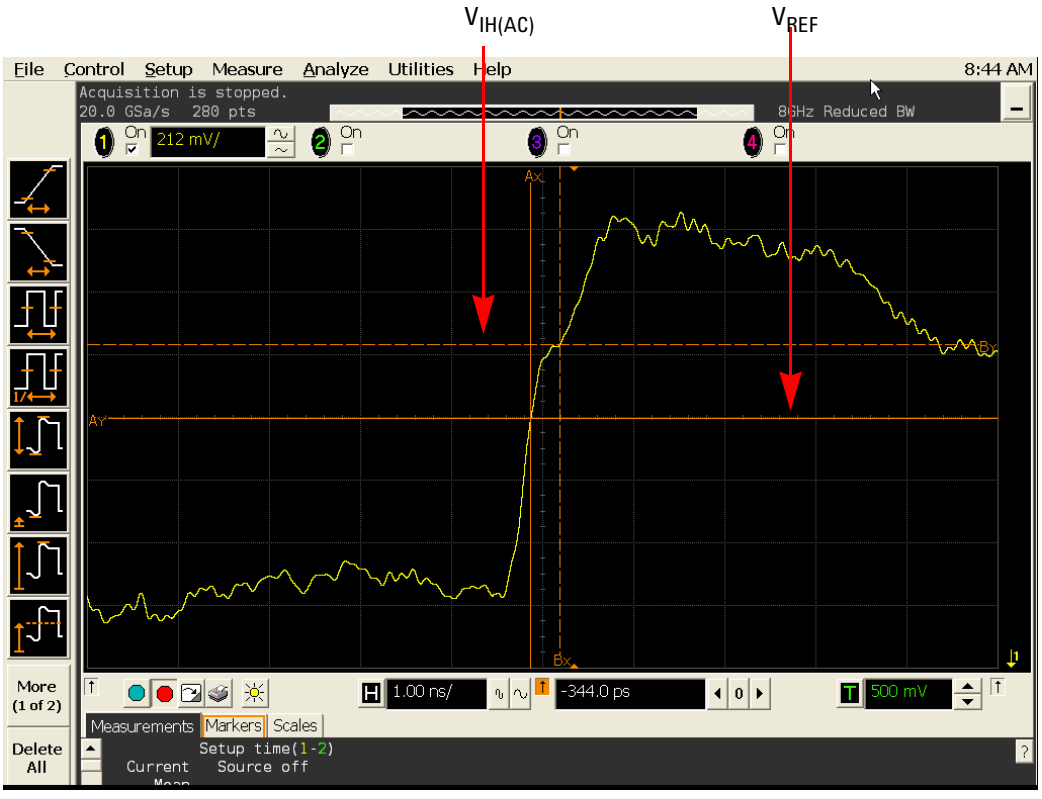


**Figure 5** $Slew_R$ in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 3** Input Slew Rate for DQ, DQS and DM

| AC Characteristics - Parameter | Symbol | DDR 400 | | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC) | DCSlew | 0.5 | 4.0 | 0.5 | 4.0 | 0.5 | 4.0 | 0.5 | 4.0 | V/ns | a, m |

NOTE a and m: Please refer to the *JEDEC Standard JESD79E*.

## PASS Condition

$\geq \mathrm{SLEW}_R$

The calculated Rising Slew value for the test signal should be greater than or equal to the SLEW value.

## Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR1 speed grade.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Calculate the number of sampling points according to the time scale value.

4 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

5 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Verify that $V_{REF}$ and $V_{IH(AC)}$ points can be found on the oscilloscope screen.

9 Calculate the delta TR.

10 Calculate Rising Slew.

$$\text{RisingSlew} = \frac{V_{IH(ac)}\text{min} - V_{REF}}{\Delta TR}$$

11 Compare test results against the compliance test limit.

## Test References

See Table 13 - Input Slew Rate for DQ, DQS, and DM, in the *JEDEC Standard JESD79E*.

# $Slew_F$ Test Method of Implementation

$Slew_F$ - Input Signal Minimum Slew Rate (Falling). The purpose of this test is to verify that the falling slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the *JEDEC Standard JESD79E*.

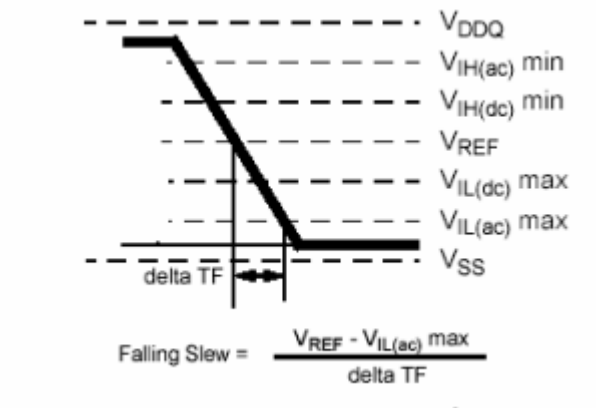


**Figure 6** $Slew_F$

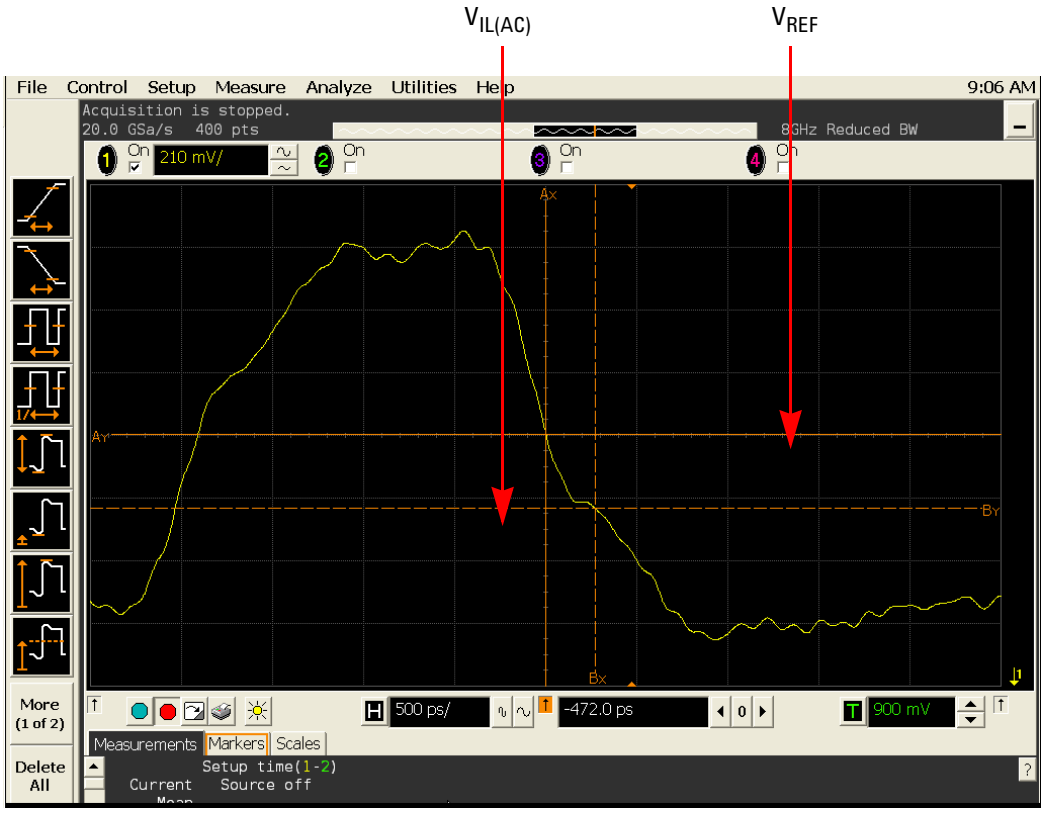


**Figure 7** $Slew_F$ in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 4** Input Slew Rate for DQ, DQS and DM

| AC Characteristics - Parameter | Symbol | DDR 400 | | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC) | DCSlew | 0.5 | 4.0 | 0.5 | 4.0 | 0.5 | 4.0 | 0.5 | 4.0 | V/ns | a, m |

NOTE a and m: Please refer to the *JEDEC Standard JESD79E*.

## PASS ConditionPASS Condition

$\geq \mathrm{SLEW}_F$

The calculated Rising Slew value for the test signal should be greater than or equal to the SLEW value.

## Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR1 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Calculate the number of sampling points according to the time scale value.

4 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

5 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on DQ-DQS to make sure it can be triggered during Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Verify that $V_{REF}$ and $V_{IL(AC)}$ points can be found on the oscilloscope screen.

9 Calculate the delta TR.

10 Calculate the Falling Slew.

$$\text{FallingSlew} = \frac{V_{REF} - V_{IL(ac)}\text{max}}{\Delta TF}$$

11 Compare test results against the compliance test limit.

## Test References

See Table 13 - Input Slew Rate for DQ, DQS, and DM, in the *JEDEC Standard JESD79E*.

# $V_{IH(AC)}$ Test Method of Implementation

$V_{IH}$ Input Logic High Test can be divided into two sub tests - $V_{IH(AC)}$ test and $V_{IH(DC)}$ test.

$V_{IH(AC)}$ - Maximum AC Input Logic High. The purpose of this test is to verify that the maximum high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limit of the $V_{IH(AC)}$ value specified in the *JEDEC Standard JESD79E*. For low power devices, the measured value must fall in between the conformance limits.

The default value of $V_{REF}$ and $V_{DDQ}$ which directly affects the conformance lower limit is as shown in Table 5. However, users have the flexibility to change this value.

**Table 5** The default value of $V_{REF}$ and $V_{DDQ}$

| Speed | DDR 200, 266, 333 | DDR 400 | Low Power |
|---|---|---|---|
| $V_{DDQ}$ | 2.50 V | 2.60 V | 1.80 V |
| $V_{REF}$ | 1.25 V | 1.30 V | 0.90 V |


**Figure 8** $V_{IH(AC)}$ Test - Maximum AC Input Logic High in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 6** AC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | $V_{IH(AC)}$ | $V_{REF}$ + 0.31 | - | V |

**Table 7** Low Power DDR SDRAM Electrical Characteristics

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| AC Input High Voltage | $V_{IHD(AC)}$ | 0.8 * $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V |
| Input High Voltage | $V_{IH}$ | 0.8 * $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V |

## PASS Condition

The maximum value for the high level voltage should be greater than or equal to the minimum $V_{IH(AC)}$ value.

For the low power device, the value must be greater than the minimum conformance limit and less than the maximum conformance limit or equal to either one conformance limit.

## Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR1 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Max** value as the test result for $V_{IH(AC)}$.
9. When multiple trials are performed, the smallest value (worst case) among the trials will be used as the test result for $V_{IH(AC)}$.
10. Compare the test results against the compliance test limits.

## Test References

See Table 7 - AC Operating Conditions and Table 8 - Low Power DDR SDRAM Electrical Characteristics, in the *JEDEC Standard JESD79E*.

# $V_{IH(DC)}$ Test Method of Implementation

$V_{IH(DC)}$ - Minimum DC Input Logic High. The purpose of this test is to verify that the minimum high level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IH(DC)}$ value specified in the *JEDEC Standard JESD79E*.

The default value of $V_{REF}$, $V_{DD}$ and $V_{DDQ}$ is as shown in Table 8. However, users have the flexibility to change this value.

**Table 8** The default value of $V_{REF}$, $V_{DD}$ and $V_{DDQ}$

| Speed | DDR 200, 266, 333 | DDR 400 | Low Power |
|---|---|---|---|
| $V_{DDQ}$ | 2.50 V | 2.60 V | 1.80 V |
| $V_{DD}$ | 2.50 V | 2.60 V | 1.80 V |
| $V_{REF}$ | 1.25 V | 1.30 V | 0.90 V |

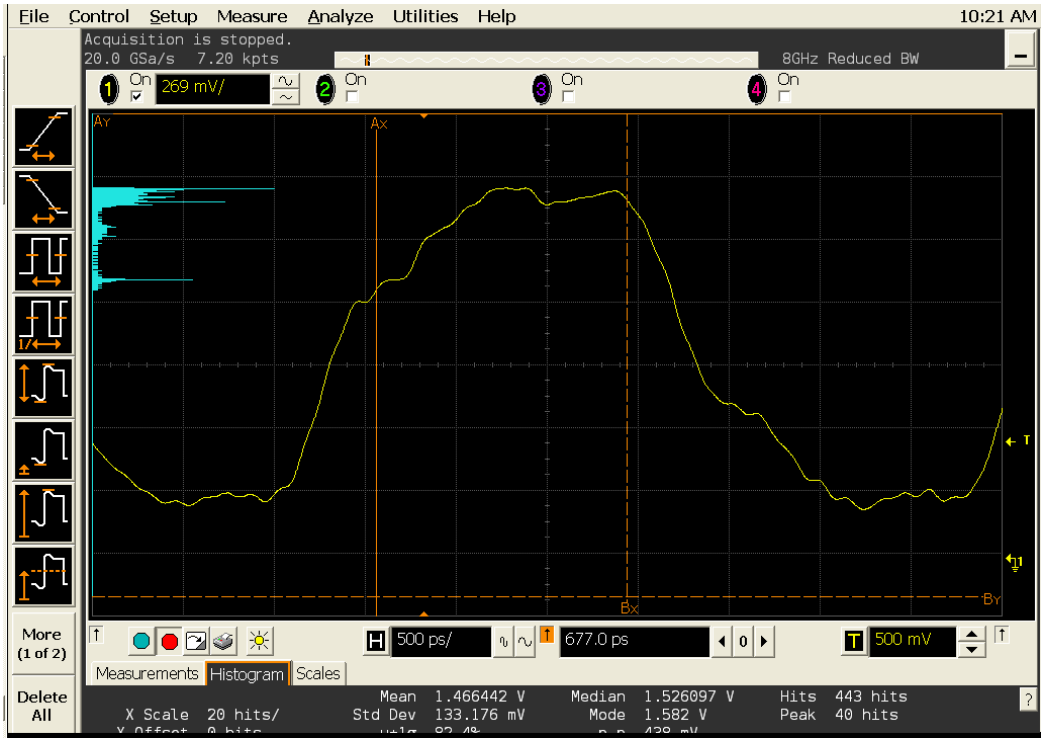


**Figure 9** $V_{IH(DC)}$ Test - Minimum DC Input Logic High in Infiniium oscilloscope.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR (Note: Address is not included in the Low Power)
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 9** Electrical Characteristics and DC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input High (Logic 1) Voltage | $V_{IH(DC)}$ | $V_{REF}$ + 0.15 | $V_{DD}$ + 0.3 | V |

**Table 10** Low Power DDR SDRAM Electrical Characteristics

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| DC Input High Voltage | $V_{IHD(DC)}$ | 0.7 * $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V |
| Input High Voltage | $V_{IH}$ | 0.8 * $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V |

## PASS Condition

The minimum value for the high level voltage should be greater than or equal to the minimum $V_{IH(DC)}$ value.

The minimum value for the high level voltage should be less than or equal to the maximum $V_{IH(DC)}$ value.

## Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR1 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Calculate the number of sampling points according to the time scale value.

4 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

5 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Use the histogram **Min** value as the test result for $V_{IH(DC)}$.

9 When multiple trials are performed, the smallest value (worst case) among the trials will be used as the test result for $V_{IH(DC)}$.

10 Compare the test results against the compliance test limits.

## Test References

See Table 6- Electrical Characteristics and DC Operating Conditions and Table 8 - Low Power DDR SDRAM Electrical Characteristics, in the *JEDEC Standard JESD79E*.

# $V_{IL(AC)}$ Test Method of Implementation

$V_{IL}$ AC Input Logic Low High Test can be divided into two sub tests: $V_{IL(AC)}$ test and $V_{IL(DC)}$ test.

$V_{IL(AC)}$ - Minimum AC Input Logic Low. The purpose of this test is to verify that the minimum low level voltage value of the test signal is lower than the conformance maximum limit of the $V_{IL(AC)}$ value specified in the *JEDEC Standard JESD79E*. For low power devices, the measured value must fall in between the conformance limits.

The default value of $V_{REF}$ and $V_{DDQ}$ is as shown in Table 11. However, users have the flexibility to change this value.

**Table 11** The default value of $V_{REF}$ and $V_{DDQ}$

| Speed | DDR 200, 266, 333 | DDR 400 | Low Power |
|---|---|---|---|
| $V_{DDQ}$ | 2.50 V | 2.60 V | 1.80 V |
| $V_{REF}$ | 1.25 V | 1.30 V | 0.90 V |

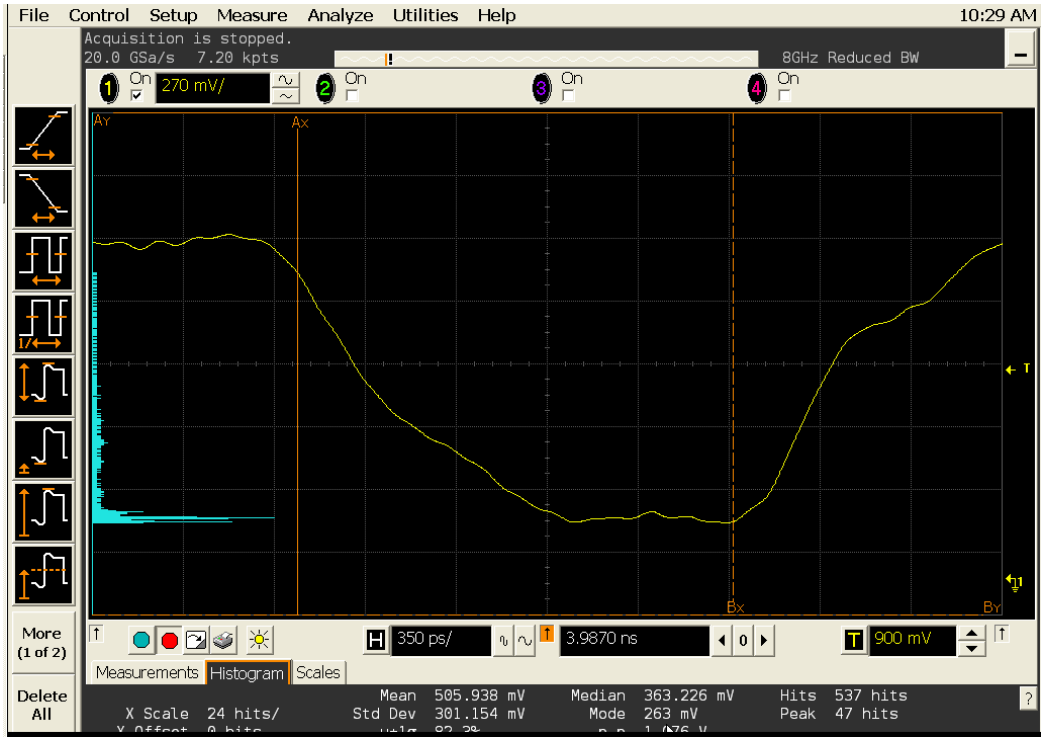


**Figure 10** $V_{IL(AC)}$ Test - Minimum AC Input Logic Low in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 12** AC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | $V_{IL(AC)}$ | $V_{REF}$ -0.31 | - | V |

**Table 13** Low Power DDR SDRAM Electrical Characteristics

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| AC Input Low Voltage | $V_{ILD(AC)}$ | -0.3 | 0.2 * $V_{DDQ}$ | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | 0.2 * $V_{DDQ}$ | V |

## PASS Condition

The minimum value for the low level voltage should be less than or equal to the maximum $V_{IL(AC)}$ value.

For the low power device, the minimum value must be greater than the minimum conformance limits.

## Measurement Algorithm

1. Calculate initial time scale value based on the selected DDR1 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurements to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Min** value as the test result for $V_{IL(AC)}$.
9. When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{IL(AC)}$.
10. Compare the test results against the compliance test limit.

## Test References

See Table 7 - AC Operating Conditions and Table 8 - Low Power DDR SDRAM Electrical Characteristics, in the *JEDEC Standard JESD79E*.

# $V_{IL(DC)}$ Test Method of Implementation

$V_{IL(DC)}$ - Maximum DC Input Logic Low. The purpose of this test is to verify that the maximum low level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IL(DC)}$ value specified in the *JEDEC Standard JESD79E*.

The default value of $V_{REF}$ and $V_{DDQ}$ is as shown in Table 14. However, users have the flexibility to change this value.

**Table 14** The default value of $V_{REF}$ and $V_{DDQ}$

| Speed | DDR 200, 266, 333 | DDR 400 | Low Power |
|---|---|---|---|
| $V_{DDQ}$ | 2.50 V | 2.60 V | 1.80 V |
| $V_{REF}$ | 1.25 V | 1.30 V | 0.90 V |

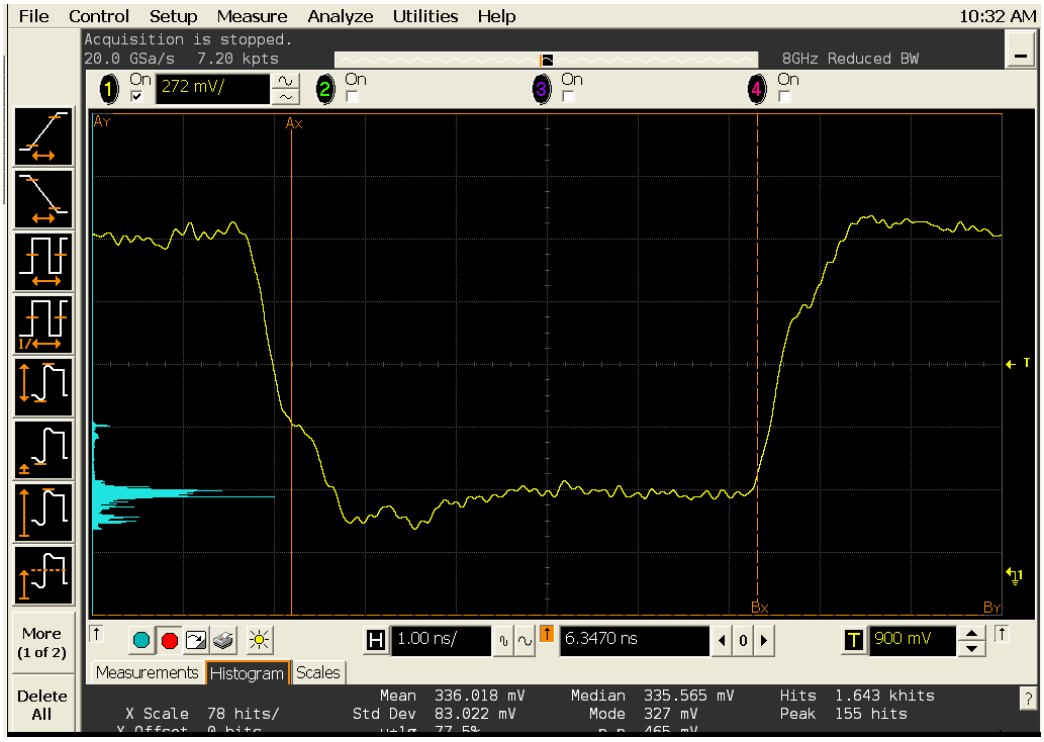


**Figure 11** $V_{IL(DC)}$ Test - Maximum DC Input Logic Low in Infiniium oscilloscope.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 15** Electrical Characteristics and DC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input Low (Logic 1) Voltage | $V_{IL(DC)}$ | -0.3 | $V_{REF}$ - 0.15 | V |

**Table 16** Low Power DDR SDRAM Electrical Characteristics

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| DC Input Low Voltage | $V_{ILD(DC)}$ | -0.3 | 0.3 * $V_{DDQ}$ | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | 0.3 * $V_{DDQ}$ | V |

## PASS Condition

The maximum value for the low level voltage should be less than or equal to the maximum $V_{IL(DC)}$ value.

The maximum value for the low level voltage should be greater than or equal to the minimum $V_{IL(DC)}$ value.

## Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR1 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Max** value as the test result for $V_{IL(DC)}$.
9. When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for $V_{IL(DC)}$.
10. Compare the test results against the compliance test limits.

## Test References

See Table 6- Electrical Characteristics and DC Operating Conditions and Table 8 - Low Power DDR SDRAM Electrical Characteristics, in the *JEDEC Standard JESD79E*.

# 4 Single-Ended Signals AC Output Parameters Tests



This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Output tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

# Probing for Single-Ended Signals AC Output Parameters Tests

When performing the Single-Ended Signals AC Output Parameters tests, the DDR1 Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Output Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR1 Compliance Test Application for the exact number of probe connections.

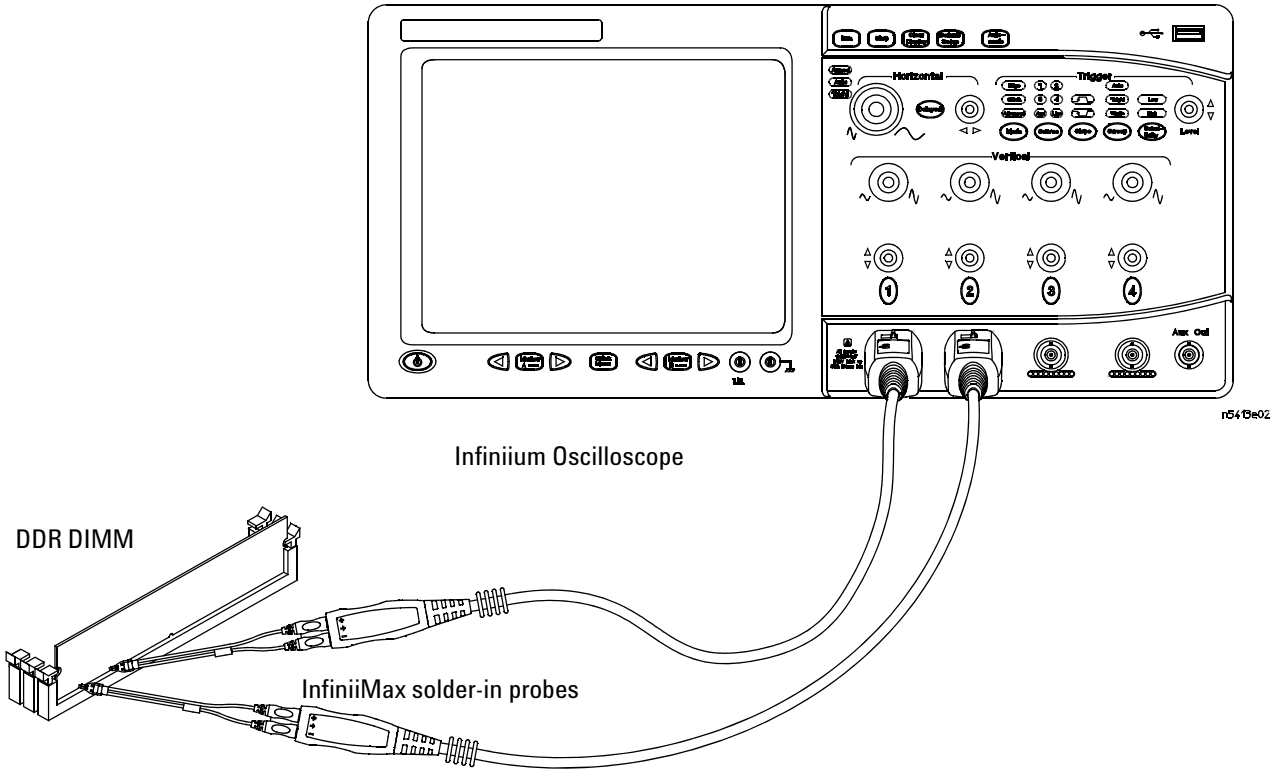


**Figure 12** Probing for Single-Ended Signals AC Output Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channels shown in Figure 12 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1. Start the automated test application as described in “Starting the DDR1 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR1 Test Application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR1-200, DDR1-266, DDR1-333, DDR1-400.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

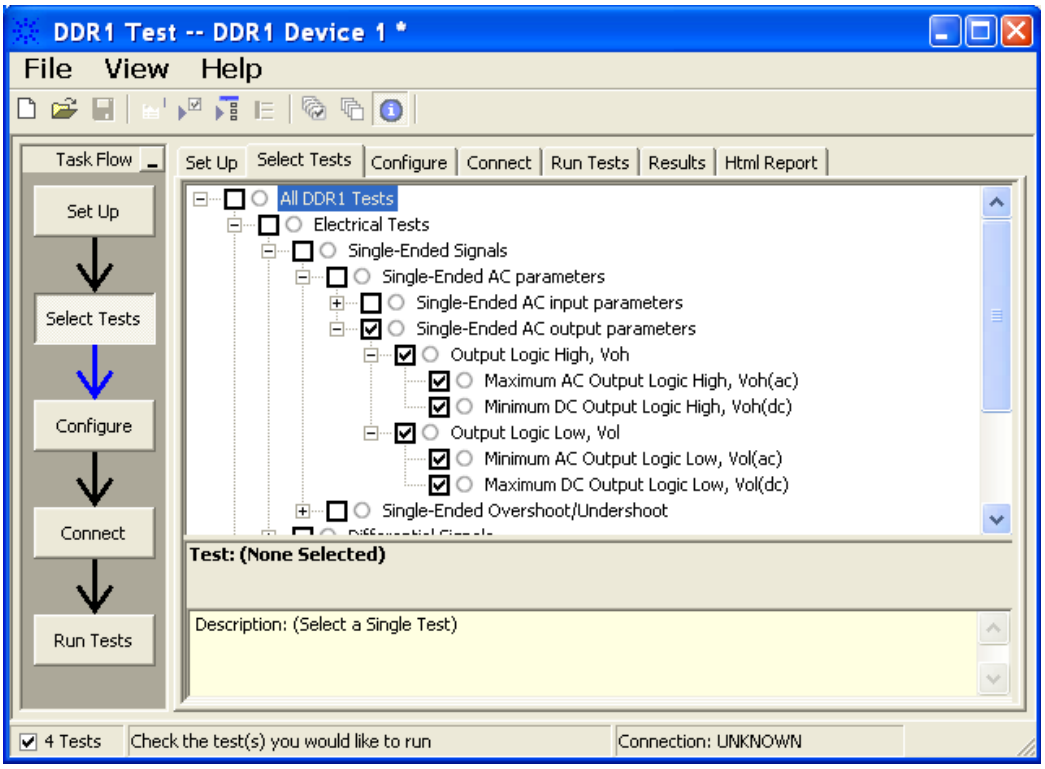


**Figure 13** Selecting Single-Ended Signals AC Output Parameters Tests

**9** Follow the DDR1 Test Application's task flow to set up the configuration options (see Table 17), run the tests and view the tests results.

**Table 17** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials. |
| Signal Threshold setting by percentage | This option allows you to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **InfiniiScan Limits** | |
| **Read Cycle** | |
| IScan_UL_READ | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle) |
| IScan_LL_READ | Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle) |
| **Write Cycle** | |
| IScan_UL_WRITE | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle) |
| IScan_LL_WRITE | Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle) |
| **Single-Ended Signals** | |
| **Single-Ended AC Parameters** | |
| Pin Under Test, PUT | Identifies the Pin Under Test for Single-Ended AC parameters. |
| PUT Source | Identifies the source of the PUT to be analyzed for Single-Ended AC tests. |
| Supporting Pin | Identifies the required supporting pin for Single-Ended AC parameters. |
| Supporting Pin Source | Identifies the source of the supporting pin for Single-Ended AC Tests. |

# $V_{OH(AC)}$ Test Method of Implementation

$V_{OH(AC)}$ - Maximum AC Output Logic High. This test is only applied to Low Power DDR SDRAM. The purpose of this test is to verify that the maximum high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limit of the $V_{OH(AC)}$ value specified in the *JEDEC Standard JESD79E*.

The default value of $V_{DDQ}$ is as shown in Table 18. However, users have the flexibility to change this value.

**Table 18** The default value of $V_{DDQ}$

| Speed | DDR 200, 266, 333 | DDR 400 | Low Power |
|---|---|---|---|
| $V_{DDQ}$ | 2.50 V | 2.60 V | 1.80 V |


**Figure 14** $V_{OH(AC)}$ Test - Maximum AC Output Logic High in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal

- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 19** Low Power DDR SDRAM Electrical Characteristics

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DC Output High Voltage (IOH = -0.1mA) | VOH | 0.9 * VDDQ | | V | - |

## PASS Condition

The maximum value for the high level voltage should be greater than or equal to the minimum $V_{OH(AC)}$ value.

## Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR1 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.

8 Use the histogram **Max** value as the test result for $V_{OH(AC)}$.

9 When multiple trials are performed, the smallest value (worst case) among the trials will be used as the test result for $V_{OH(AC)}$.

10 Compare the test results against the compliance test limits.

## Test References

See Table 8 - Low Power DDR SDRAM Electrical Characteristics, in the *JEDEC Standard JESD79E*.

# $V_{OL(AC)}$ Test Method of Implementation

$V_{OL(AC)}$ - Minimum AC Output Logic Low. This test is only applied to Low Power DDR SDRAM. The purpose of this test is to verify that the minimum low level voltage value of the test signal is lower than the conformance maximum limit of the $V_{OL(AC)}$ value specified in the *JEDEC Standard JESD79E*.

The default value of $V_{DDQ}$ is as shown in Table 20. However, users have the flexibility to change this value.

**Table 20** The default value of $V_{DDQ}$

| Speed | DDR 200, 266, 333 | DDR 400 | Low Power |
|---|---|---|---|
| $V_{DDQ}$ | 2.50 V | 2.60 V | 1.80 V |

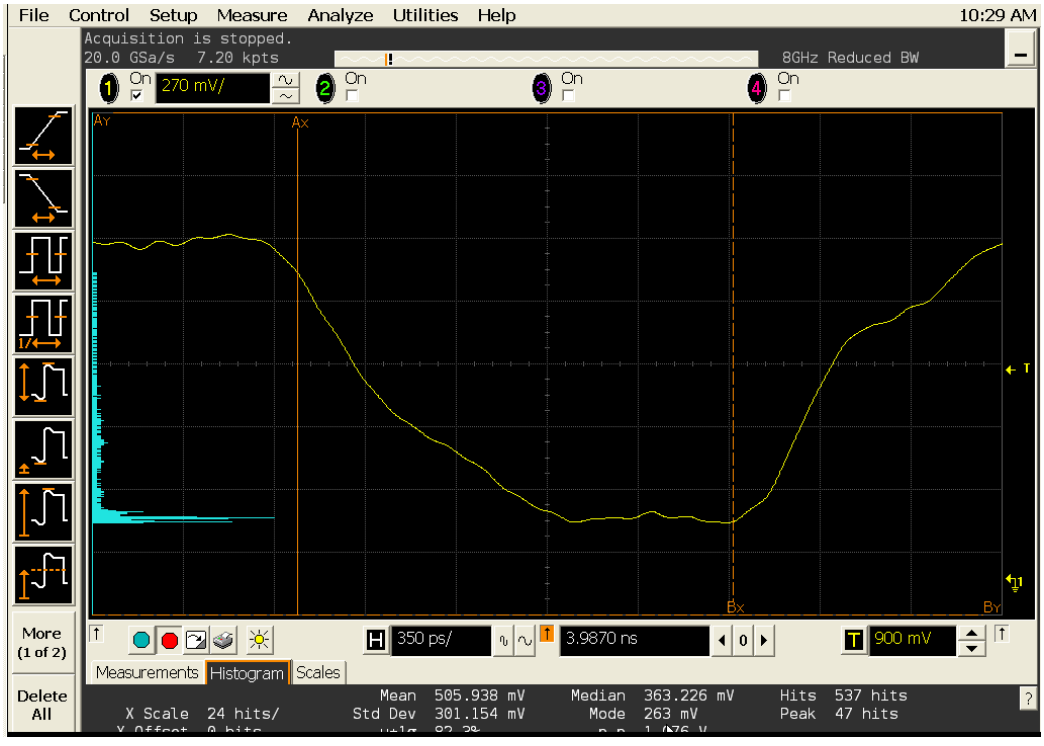


**Figure 15** $V_{OL(AC)}$ Test - Minimum AC Output Logic Low in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 21** Low Power DDR SDRAM Electrical Characteristics

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DC Output Low Voltage (IOL = -0.1mA) | VOL | - | 0.1 * VDDQ | V | - |

## PASS Condition

The minimum value for the low level voltage should be less than or equal to the maximum $V_{OL(AC)}$ value.

## Measurement Algorithm

1. Calculate initial time scale value based on the selected DDR1 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurements to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Use the histogram **Min** value as the test result for $V_{OL(AC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{OL(AC)}$.

10 Compare the test results against the compliance test limits.

## Test References

See Table 8 - Low Power DDR SDRAM Electrical Characteristics, in the *JEDEC Standard JESD79E*.

# 5 Single-Ended Signals Overshoot/Undershoot Tests



This section provides the Methods of Implementation (MOIs) for Single-Ended Signals Overshoot/Undershoot tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

## Probing for Overshoot/Undershoot Tests

When performing the Single-Ended Signals Overshoot/Undershoot tests, the DDR1 Compliance Test Application will prompt you to make the proper connections as shown in the following diagram. Refer to the Connection tab in DDR1 Compliance Test Application for the exact number of probe connections.

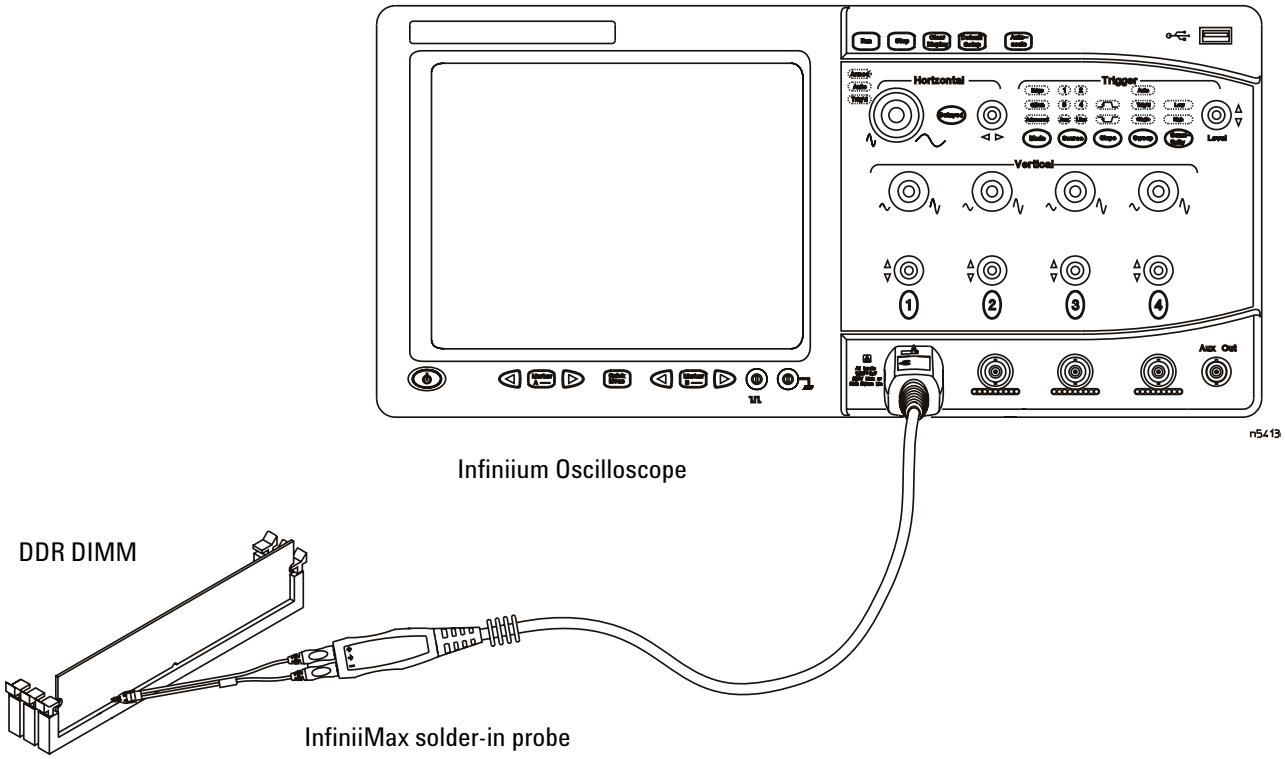


**Figure 16** Probing for Single-Ended Signals Overshoot/Undershoot Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channel shown in Figure 16 is just an example).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1. Start the automated test application as described in “Starting the DDR1 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR1 Test Application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR1-200, DDR1-266, DDR1-333, DDR1-400.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

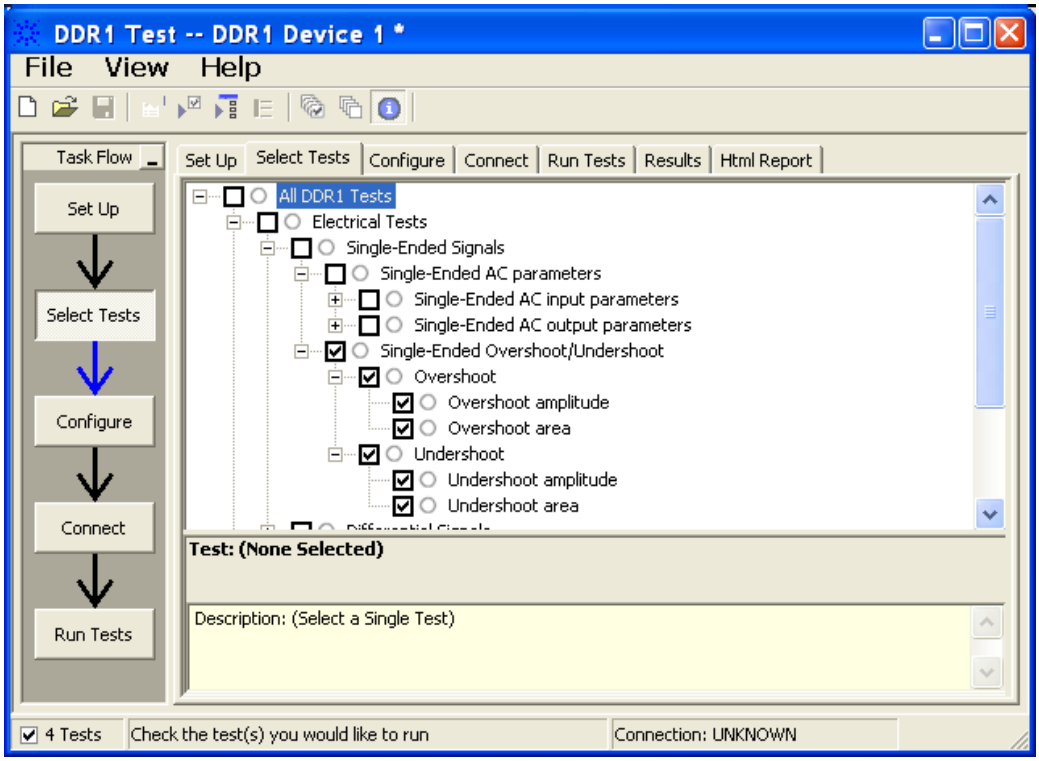


**Figure 17** Selecting Single-Ended Signals Overshoot/Undershoot Tests

9 Follow the DDR1 Test Application's task flow to set up the configuration options (see Table 22), run the tests and view the tests results.

**Table 22** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **InfiniiScan Limits** | |
| **Read Cycle** | |
| IScan_UL_READ | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle) |
| IScan_LL_READ | Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle) |
| **Write Cycle** | |
| IScan_UL_WRITE | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle) |
| IScan_LL_WRITE | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle) |
| **Single-Ended Signals** | |
| **Single-Ended Overshoot/Undershoot** | |
| Pin Under Test, PUT | Identifies the Pin Under Test for Single-Ended Overshoot/Undershoot. |
| PUT Source | Identifies the source of the PUT to be analyzed for Single-Ended AC tests. |

## AC Overshoot Test Method of Implementation

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area. The purpose of this test is to verify that the overshoot value of the test signal is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the *JEDEC Standard JESD79E*.

When there is an overshoot, the area is calculated based on the overshoot width. The Overshoot area should be lower than or equal to the conformance limit of the maximum Overshoot area allowed as specified in the *JEDEC Standard JESD79E*.

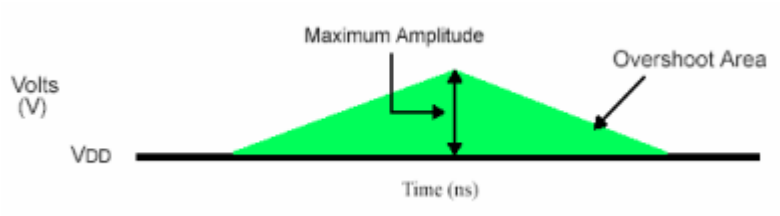


**Figure 18** AC Overshoot

## Signals of Interest

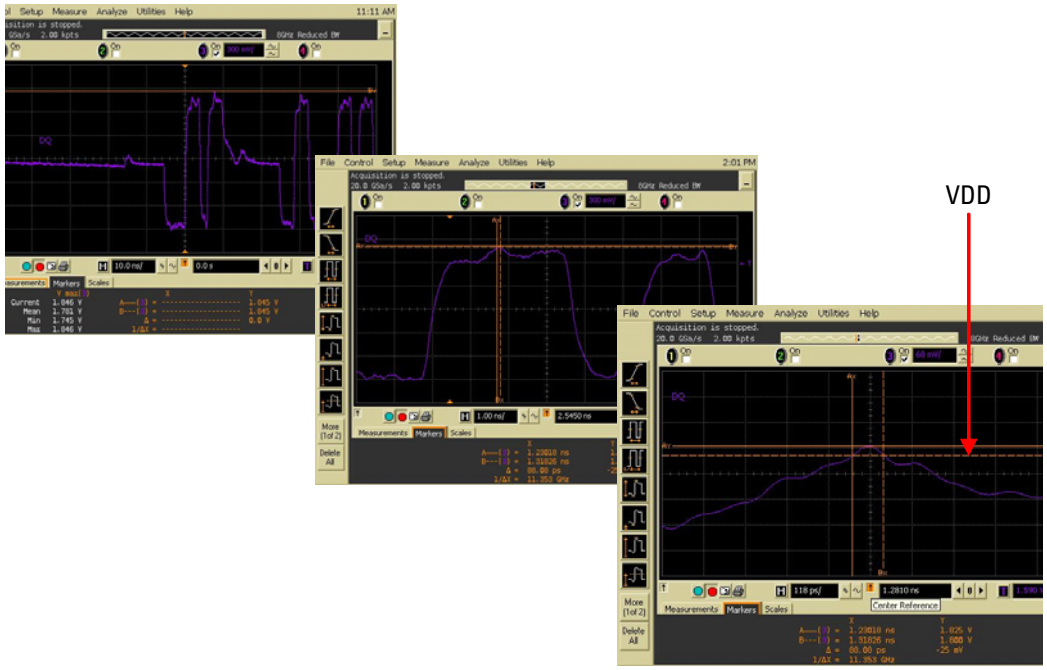


**Figure 19** AC Overshoot in Infiniium oscilloscope

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 23** AC Overshoot/Undershoot Specification for Address and Control Pins

| Parameter | Specification | |
|---|---|---|
| | DDR 333 | DDR 200/266 |
| Maximum peak amplitude allowed for overshoot | TBD | 1.5 V |
| Maximum peak amplitude allowed for undershoot | TBD | 1.5 V |
| The area between the overshoot signal and VDD must be less than or equal to | TBD | 4.5 V-ns |
| The area between the undershoot signal and GND must be less than or equal to | TBD | 4.5 V-ns |

**Table 24** AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

| Parameter | Specification | |
|---|---|---|
| | DDR 333 | DDR 200/266 |
| Maximum peak amplitude allowed for overshoot | TBD | 1.2 V |
| Maximum peak amplitude allowed for undershoot | TBD | 1.2 V |
| The area between the overshoot signal and VDD must be less than or equal to | TBD | 2.4 V-ns |
| The area between the undershoot signal and GND must be less than or equal to | TBD | 2.4 V-ns |

## PASS Condition

The measured maximum voltage value can be less than or equal to the maximum overshoot value.

The calculated Overshoot area value can be less than or equal to the maximum Overshoot area allowed.

## Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate initial time scale value based on the number of sampling points.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Initialize the scope settings.

8 Get timestamp of maximum peak voltage on the waveform.

9 Perform manual zoom waveform to maximum peak area.

10 Get the timestamp of voltage value for VDD(-1.8 V) level closest to the peak point value in order to calculate the maximum overshoot length duration.

11 Calculate the Overshoot area (V-ns)

   a Area of calculation is based on the area of calculation of a triangle where the Overshoot width is used as the triangle base and the Overshoot amplitude is used as the triangle height.

   b Area = 0.5 * base * height.

12 When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for the Overshoot amplitude and Overshoot area. The worst case for the area might not happen during the worst case for the amplitude.

13 Compare the test results against the compliance test limits.

## Test References

See Table 20 - AC Overshoot/Undershoot Specification for Address and Control Pins, and Table 21 - AC Overshoot/Undershoot Specification for Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79E*.

## AC Undershoot Test Method of Implementation

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area. The purpose of this test is to verify that the undershoot value of the test signal is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC Standard JESD79E*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC Standard JESD79E*.

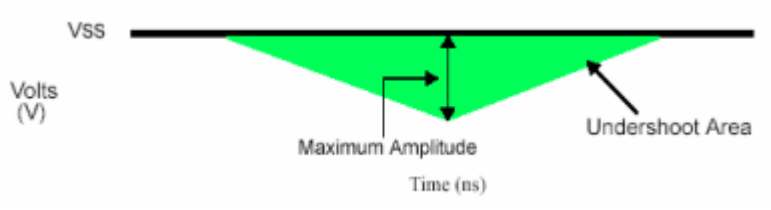


**Figure 20** AC Undershoot

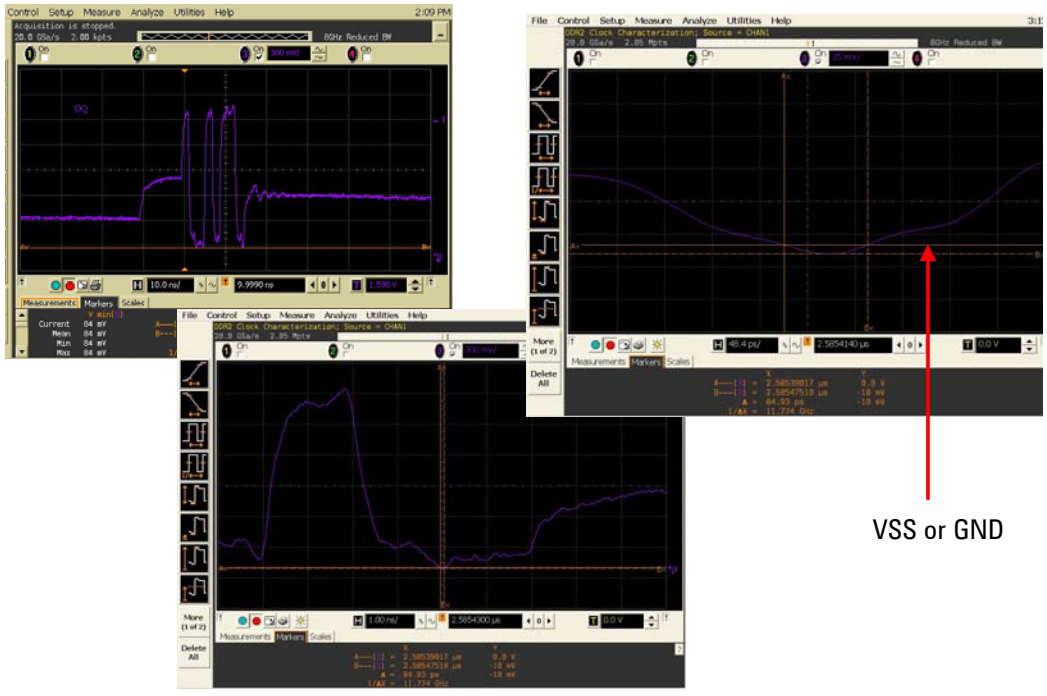


**Figure 21** AC Undershoot in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 25** AC Overshoot/Undershoot Specification for Address and Control Pins

| Parameter | Specification | |
|---|---|---|
| | DDR 333 | DDR 200/266 |
| Maximum peak amplitude allowed for overshoot | TBD | 1.5 V |
| Maximum peak amplitude allowed for undershoot | TBD | 1.5 V |
| The area between the overshoot signal and VDD must be less than or equal to | TBD | 4.5 V-ns |
| The area between the undershoot signal and GND must be less than or equal to | TBD | 4.5 V-ns |

**Table 26** AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

| Parameter | Specification | |
|---|---|---|
| | DDR 333 | DDR 200/266 |
| Maximum peak amplitude allowed for overshoot | TBD | 1.2 V |
| Maximum peak amplitude allowed for undershoot | TBD | 1.2 V |
| The area between the overshoot signal and VDD must be less than or equal to | TBD | 2.4 V-ns |
| The area between the undershoot signal and GND must be less than or equal to | TBD | 2.4 V-ns |

## PASS Condition

The measured minimum voltage value for the test signal can be less than or equal to the maximum undershoot value.

The calculated undershoot area value can be less than or equal to the maximum undershoot area allowed.

## Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate initial time scale value based on the number of sampling points.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Initialize the scope settings.
8. Get timestamp of minimum peak voltage on the waveform.
9. Perform manual zoom waveform to minimum peak area.
10. Get timestamp of voltage value for GND (0 V) level closest to the minimum peak point value in order to calculate the undershoot length duration.
11. Calculate the Undershoot area (V-ns)
    a. Area of calculation is based on the area of calculation of a triangle where the undershoot width is used as the triangle base and the undershoot amplitude is used as the triangle height.
    b. Area = 0.5 * base * height.
12. When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for the Undershoot amplitude and Undershoot area. The worst case for the area might not happen during the worst case for the amplitude.
13. Compare test results against the compliance test limits.

## Test References

See Table 20 - AC Overshoot/Undershoot Specification for Address and Control Pins, and Table 21 - AC Overshoot/Undershoot Specification for Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79E*.

# 6 Differential Signals AC Input Parameters Tests



This section provides the Methods of Implementation (MOIs) for Differential Signals AC Input tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

# Probing for Differential Signals AC Input Parameters Tests

When performing the Differential Signals AC Input Parameters tests, the DDR1 Compliance Test Application will prompt you to make the proper connections. The connection for the Differential Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR1 Compliance Test Application for the exact number of probe connections.

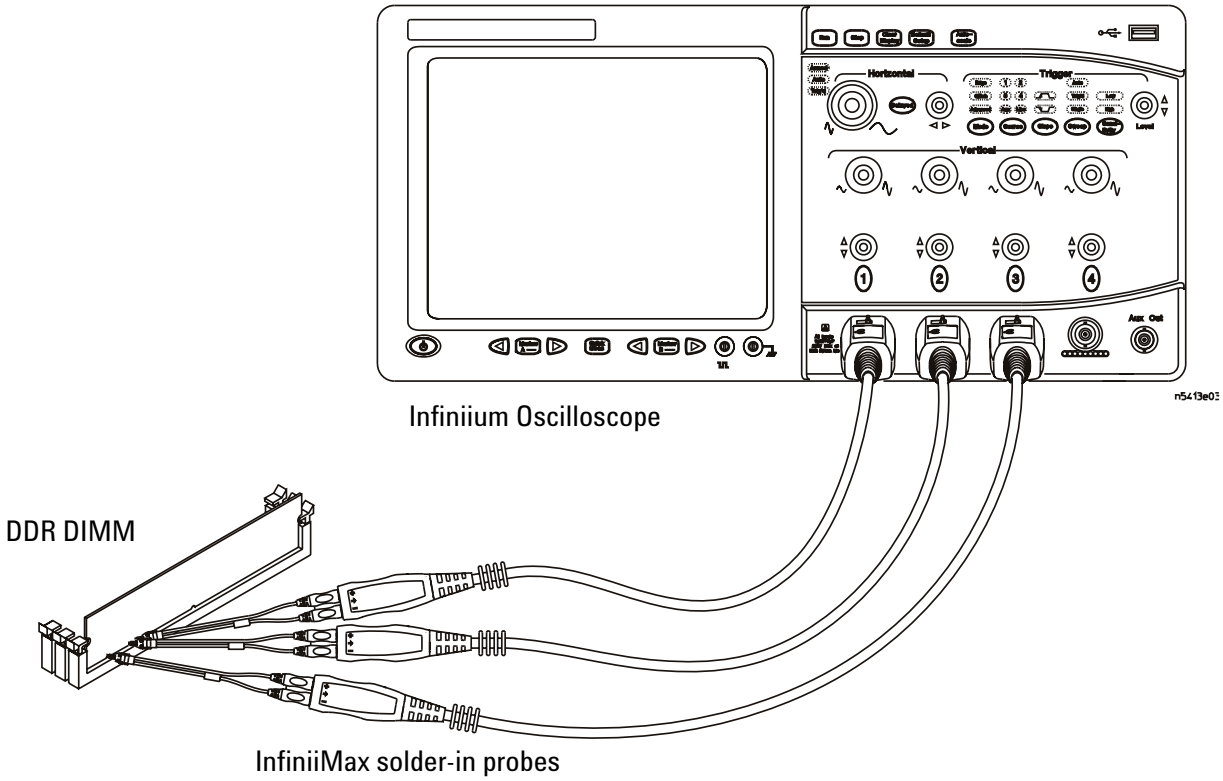


**Figure 22** Probing for Differential Signals AC Input Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channels shown in Figure 22 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1. Start the automated test application as described in “Starting the DDR1 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR1 Test Application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR1-200, DDR1-266, DDR1-333, DDR1-400.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

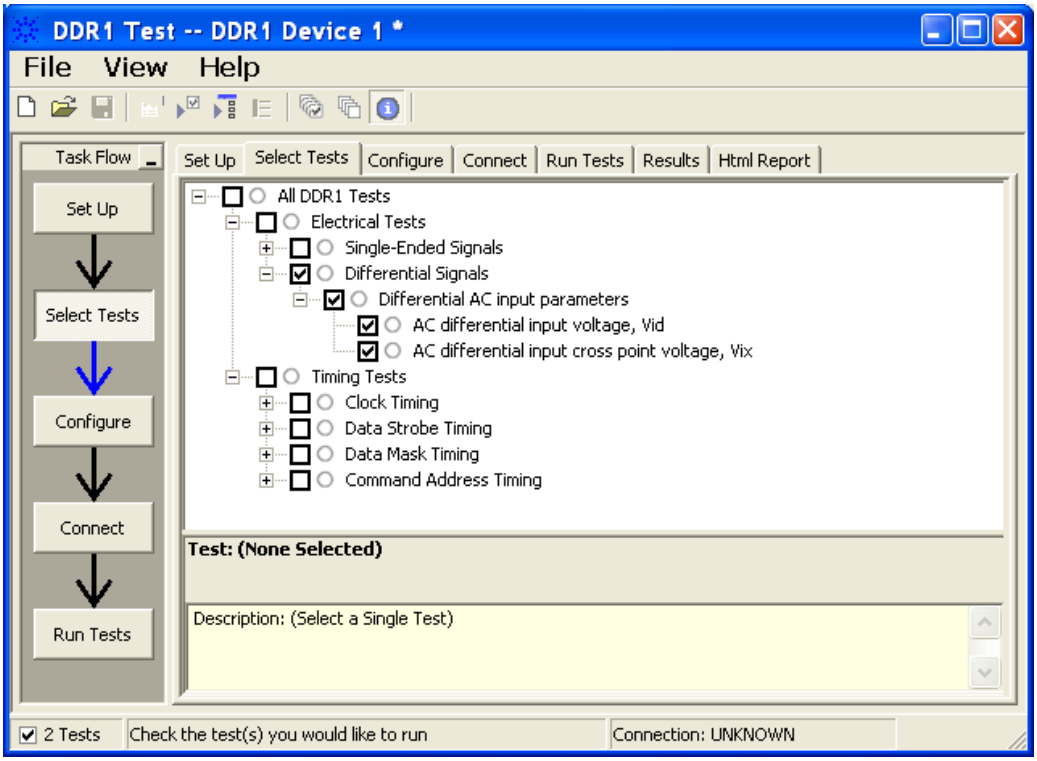


**Figure 23** Selecting Differential Signals AC Input Parameters Tests

**9** Follow the DDR1 Test Application's task flow to set up the configuration options (see Table 27), run the tests and view the tests results.

**Table 27** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **InfiniiScan Limits** | |
| **Read Cycle** | |
| IScan_UL_READ | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle) |
| IScan_LL_READ | Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle) |
| **Write Cycle** | |
| IScan_UL_WRITE | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle) |
| IScan_LL_WRITE | Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle) |
| **Differential Tests** | |
| Pin Under Test, PUT | Identifies the Pin Under Test for Differential AC parameters. |
| PUT (+) Source | Identifies the source of the PUT(+) for Differential AC tests. |
| PUT (-) Source | Identifies the source of the PUT(-) for Differential AC tests. |
| Supporting Pin | Identifies the required supporting pin for Differential AC parameters. |
| Supporting Pin Source | Identifies the source of the supporting pin for Differential AC tests. |

# $V_{ID(AC)}$, AC Differential Input Voltage - Test Method of Implementation

The purpose of this test is to verify that the magnitude difference between the differential input signals pair is within the conformance limits of the $V_{ID(AC)}$ as specified in the *JEDEC Standard JESD79E*.

The default value of $V_{DDQ}$ is as shown in Table 28. However, users have the flexibility to change this value.

**Table 28** The default value of $V_{DDQ}$

| Speed | DDR 200, 266, 333 | DDR 400 | Low Power |
|---|---|---|---|
| $V_{DDQ}$ | 2.50 V | 2.60 V | 1.80 V |

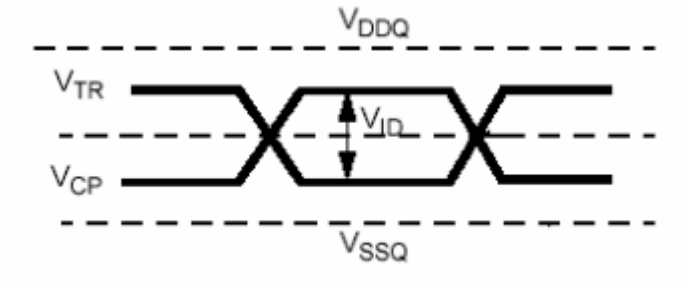


**Figure 24** $V_{ID}$ AC Differential Input Voltage

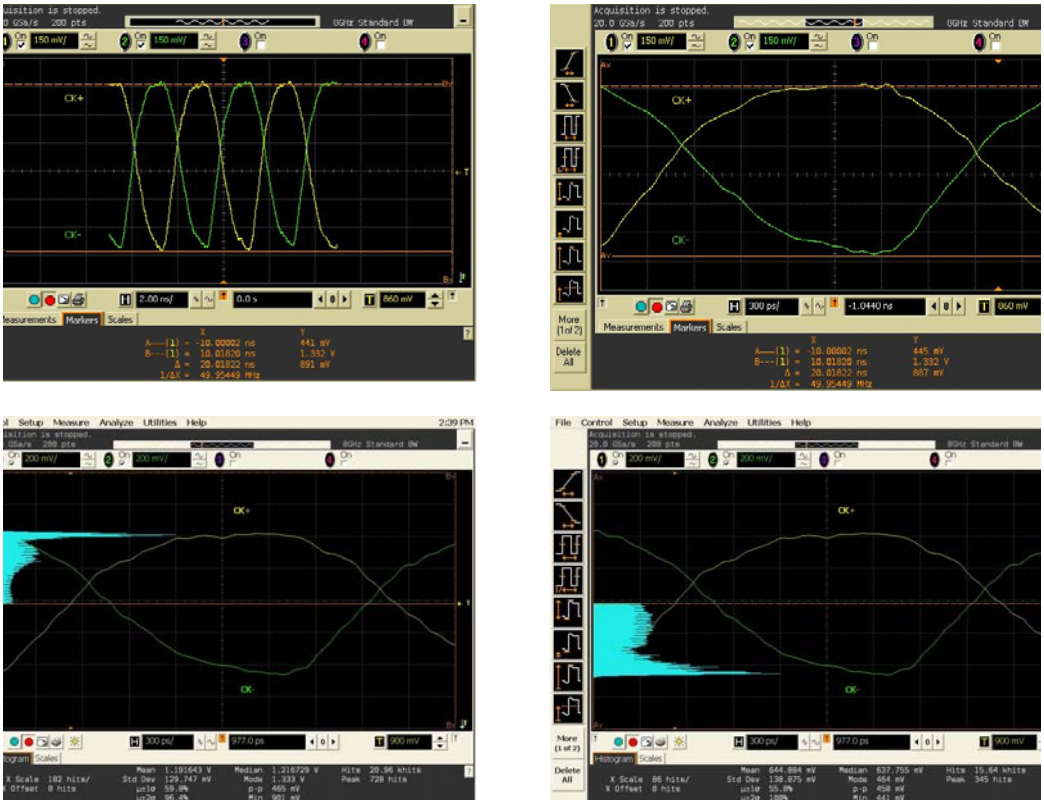


**Figure 25** $V_{ID(AC)}$ in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)*
- Data Signal (DQ as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 29** AC Operating Conditions

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Differential Voltage, CK and CK# inputs | $V_{ID(AC)}$ | 0.7 | $V_{DDQ}$ + 0.6 | V | 9 |

NOTE 9: $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on CK#.

## PASS Condition

The calculated magnitude of the differential voltage for the test signals pair can be within the conformance limits of the $V_{ID(AC)}$ value.

## Measurement Algorithm

1. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Obtain sample or acquire data waveforms, for example CK+ and CK-.
6. Use histogram function (mode value) to find the nominal high level value for CK+ and nominal low level value for CK-.
7. Subtract the CK- low level value from the CK+ high level value.
8. Compare the test results against the compliance test limits.

## Test References

See Table 7 - AC Operating Conditions, in the *JEDEC Standard JESD79E*.

# $V_{IX(AC)}$, AC Differential Input Cross Point Voltage -Test Method of Implementation

The purpose of this test is to verify the crossing point of the input differential test signals pair is within the conformance limits of the $V_{IX(AC)}$ as specified in the *JEDEC Standard JESD79E*.

The default value of $V_{DDQ}$ is as shown in Table 30. However, users have the flexibility to change this value.

**Table 30** The default value of $V_{DDQ}$

| Speed | DDR 200, 266, 333 | DDR 400 | Low Power |
|---|---|---|---|
| $V_{DDQ}$ | 2.50 V | 2.60 V | 1.80 V |

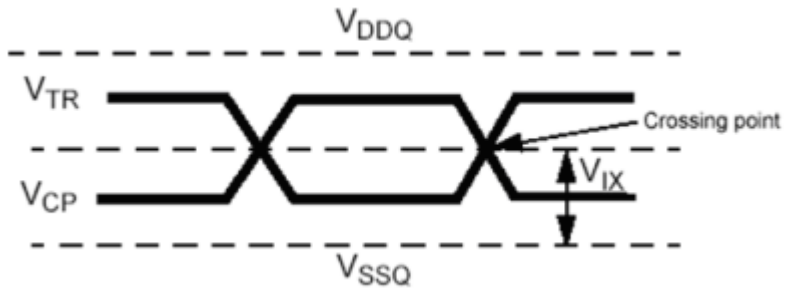


**Figure 26** $V_{IX}$ AC Differential Input Voltage

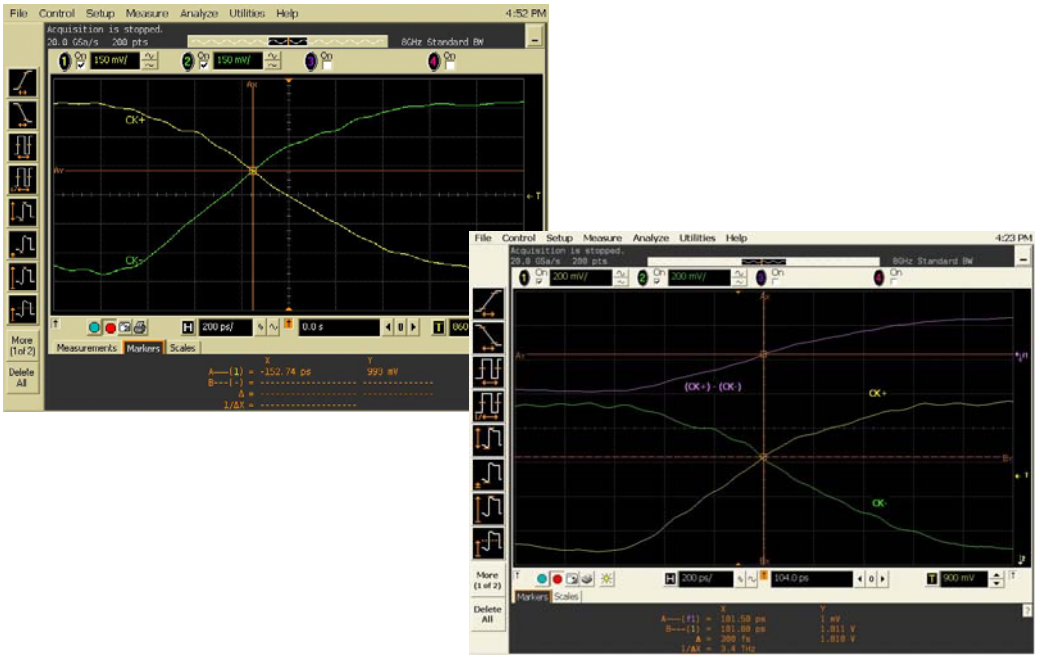


**Figure 27** $V_{IX(AC)}$ in Infiniium oscilloscope.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)*
- Data Signal (DQ as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

## Test Definition Notes from the Specification

**Table 31** AC Operating Conditions

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Differential Voltage, CK and CK# inputs | $V_{IX(AC)}$ | 0.5 * $V_{DDQ}$ - 0.2 | 0.5 * $V_{DDQ}$ + 0.2 | V | 10 |

NOTE 10: The value of $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on CK#.

## PASS Condition

The measured crossing point value for the differential test signals pair can be within the conformance limits of $V_{IX(AC)}$ value.

## Measurement Algorithm

1. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Obtain sample or acquire data waveforms, for example CK+ and CK-.
6. Generate the differential waveform from two source input.
7. Get the timestamp of voltage value = 0 V level (crossing point).
8. Get the actual crossing value using the obtained timestamp.
9. Compare the test results against the compliance test limits.

## Test References

See Table 7 - AC Operating Conditions, in the *JEDEC Standard JESD79E*.

# 7 Clock Timing (CT) Tests



This section provides the Methods of Implementation (MOIs) for Clock Timing tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

**NOTE** Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

# Probing for Clock Timing Tests

When performing the Clock Timing tests, the DDR1 Compliance Test Application will prompt you to make the proper connections. The connection for Clock Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR1 Compliance Test Application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

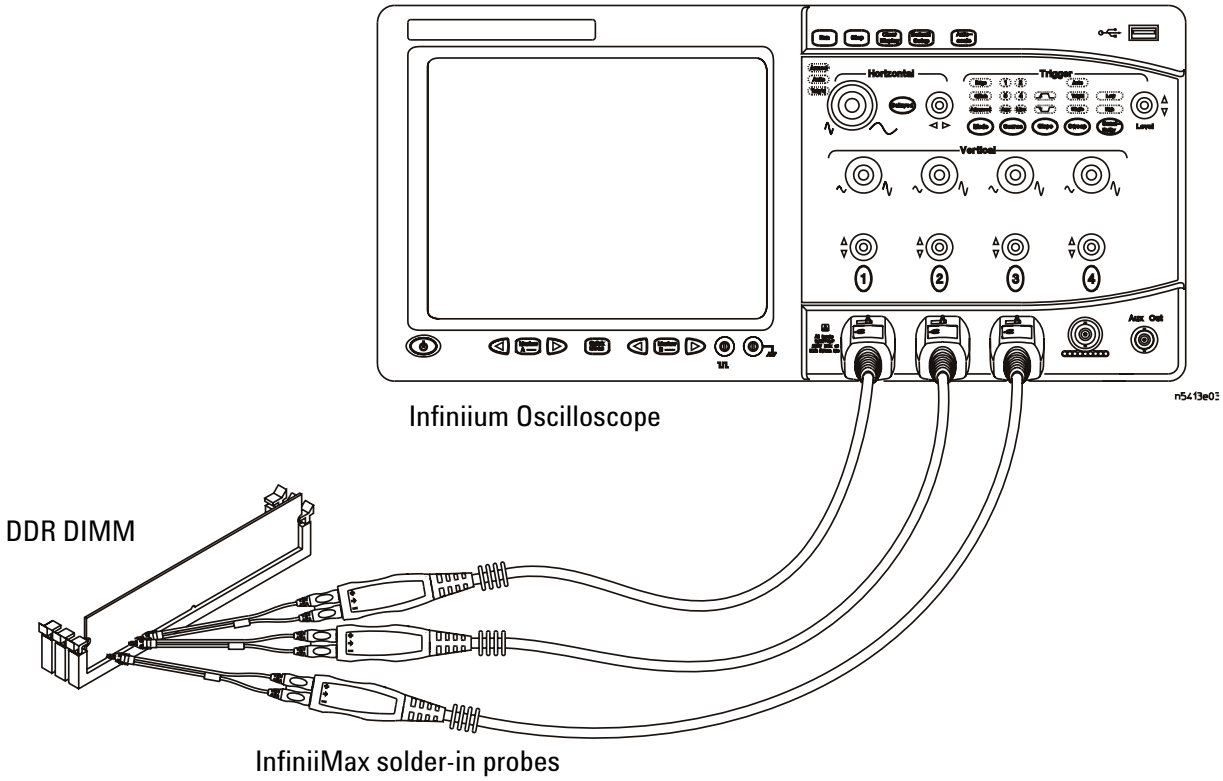


**Figure 28** Probing for Clock Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channels shown in Figure 28 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1. Start the automated test application as described in “Starting the DDR1 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR1 Test Application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR1-200, DDR1-266, DDR1-333, DDR1-400.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

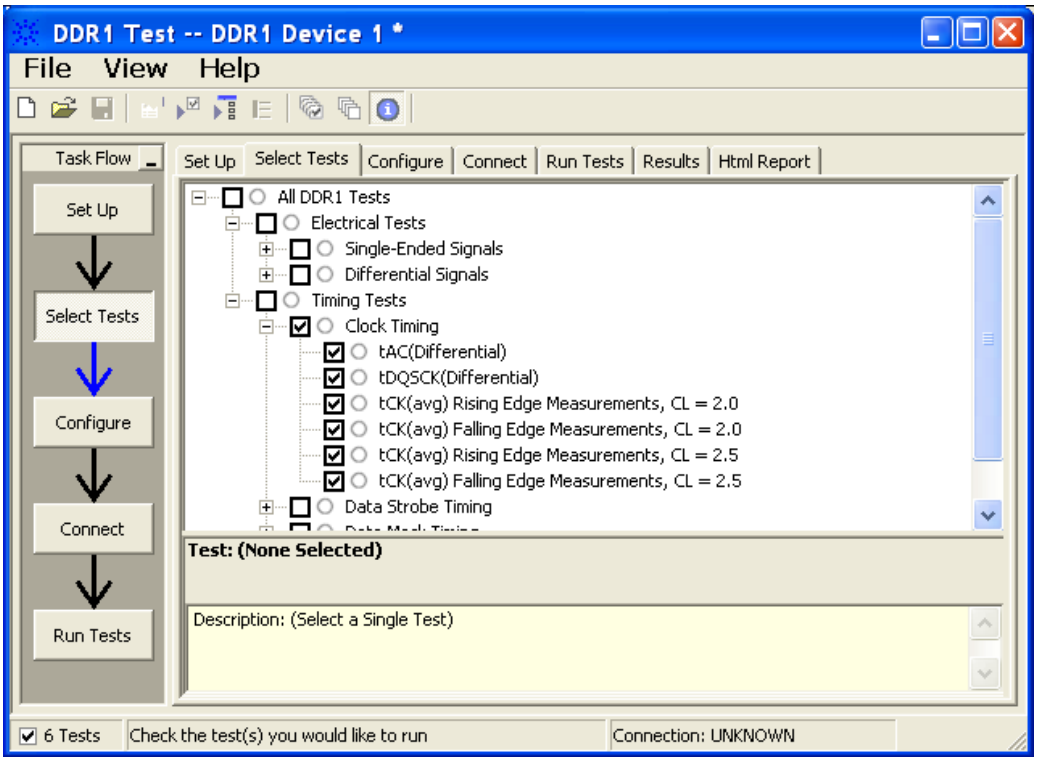


**Figure 29** Selecting Clock Timing Tests

**9** Follow the DDR1 Test Application's task flow to set up the configuration options (see Table 32), run the tests and view the tests results.

**Table 32** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **Timing Tests** | |
| Total Bit Display | Allows user to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals. |
| Verify Selected Rank Only? | If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope. |
| Channel (1,2,3) | Signal connected to the specific channel. |
| Pin Under Test, PUT | Signal used for testing. |

# tAC, DQ Output Access Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time interval from data output (DQ Rising and Falling Edge) access time to the nearest rising or falling edge of the clock must be within the conformance limit as specified in the *JEDEC Standard JESD79E*.

There is tAC(min) and tAC(max) as shown in Figure 31. From the specification, you can observe that the minimum value is at negative while the maximum is at positive.

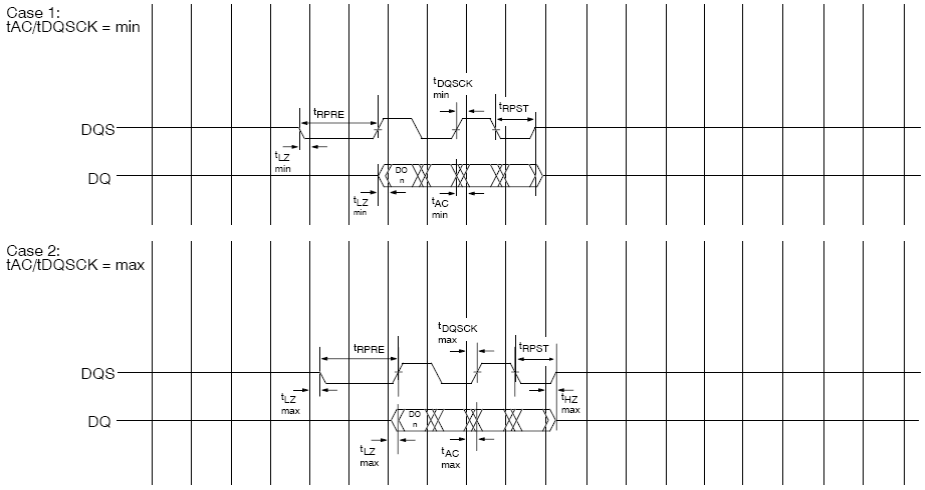


**Figure 30** DQ Output Access Time from CK/CK#

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel

## Test Definition Notes from the Specification

**Table 33** Electrical Characteristics and AC Timing

| AC Characteristics - Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ output access time from CK/$\overline{CK}$ | tAC | -0.70 | +0.70 | -0.75 | +0.75 | -0.8 | +0.8 | ns | |

| AC Characteristics - Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ output access time from CK/$\overline{CK}$ | tAC | -0.7 | +0.7 | -0.7 | +0.7 | -0.7 | +0.7 | ns | |

**Table 34** AC Timing Variations for DDR 333, DDR 266 & DDR 200 Devices

| Parameter | DDR 333B | | DDR 266A | | DDR 266B | | DDR 200 | | DDR 200B | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| tAC | -0.7 | 0.7 | -0.75 | 0.75 | -0.75 | 0.75 | -0.8 | 0.8 | -0.8 | 0.8 | ns |

## Pass Condition

The measured time interval between the data access output and the rising edge of the clock should be within the specification limits.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope setting. Verify the actual DUT speed against user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.Search for the DQS pre-amble towards the left from the point where the Read Cycle was previously captured. The For loops, TEdge and DeltaTime are used to search the pre-amble.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge# for the respective signal, begin the tAC measurement bit by bit in Read Data Burst. Begin at the 1st bit of the Read cycle, from the Read pre-amble.

11 Continue the measurement until last bit (for example, until a tristate happens, which indicates the end of a Data Burst for the respective Read Cycle).

12 DQ-Clock timing measurement compares the Rising Edge (Vih_ac OR Vil_dc against clock crossing) OR the Falling Edge (Vil_ac OR Vih_dc against clock crossing).

13 Within the data burst, measure each bit, for instance rising and falling edge of DQ-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for clock signal while marker B for data signal, for the Worst Case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing and Table 12 - AC Timing Variations For DDR 333, DDR 266 and DDR 200 Devices, in the *JEDEC Standard JESD79E*.

# tDQSCK, DQS Output Access Time from CK/CK #- Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the nearest rising or falling edge of the clock is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

There is tDQSCK(min) and tDQSCK(max) as shown in Figure 31. From the specification, you can observe that the minimum value is at negative while the maximum is at positive.

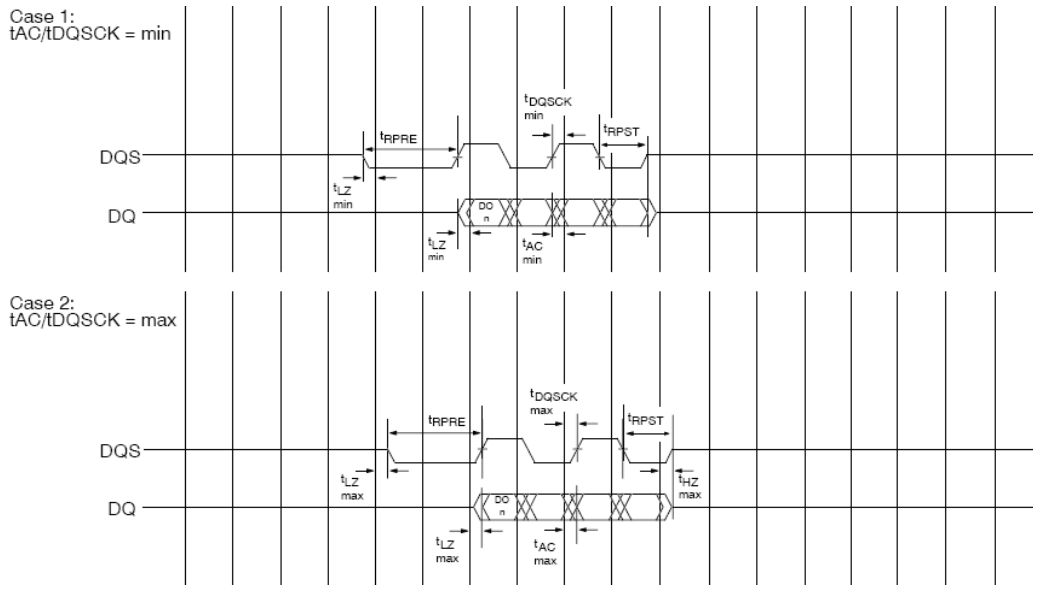


**Figure 31** DQS Output Access Time from CK/CK#

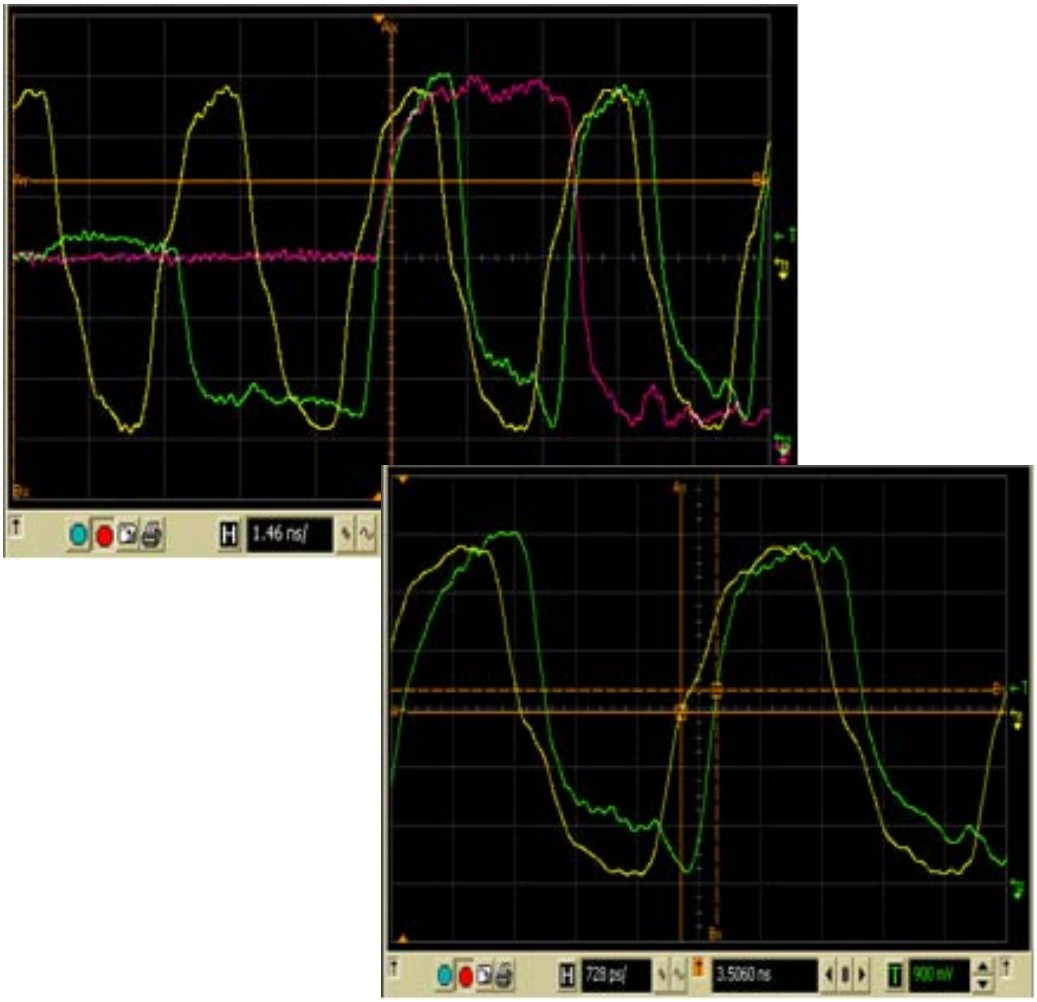


**Figure 32** tDQSCK in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 35** Electrical Characteristics and AC Timing

| AC Characteristics - Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS output access time from CK/$\overline{CK}$ | tDQSCK | -0.60 | +0.60 | -0.75 | +0.75 | -0.8 | +0.8 | ns | |

| AC Characteristics - Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS output access time from CK/$\overline{CK}$ | tDQSCK | -0.6 | +0.6 | -0.6 | +0.6 | -0.6 | +0.6 | ns | |

**Table 36** AC Timing Variations for DDR 333, DDR 266 & DDR 200 Devices

| Parameter | DDR 333B | | DDR 266A | | DDR 266B | | DDR 200 | | DDR 200B | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| tDQSCK | -0.7 | 0.7 | -0.75 | 0.75 | -0.75 | 0.75 | -0.8 | 0.8 | -0.8 | 0.8 | ns |

## PASS Condition

The measured time interval between the data strobe access output and the rising edge of the clock should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope setting. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSCK measurement bit by bit in the Read data burst. Begin at the 1st bit of the Read cycle, from the Read preamble.

11 Continue the measurement until last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).

12 The DQS-Clock timing measurement compares the rising edge (DQS crossing against clock crossing) OR the falling edge (DQS crossing against clock crossing).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing and Table 12 - AC Timing Variations For DDR 333, DDR 266 and DDR 200 Devices, in the *JEDEC Standard JESD79E*.

# Average Clock Period - tCK(avg) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. tCK(avg) is average clock period within 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window. The tCK(avg) Falling Edge Measurements measures from the falling edge to the falling edge.

## Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

## Test Definition Notes from the Specification

**Table 37** Electrical Characteristics and AC Timing

| AC Characteristics - Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock cycle time CL = 2.5 | tCK | 6 | 12 | 7.5 | 12 | 10 | 12 | ns | 30 |
| Clock cycle time CL = 2 | tCK | 7.5 | 12 | 7.5 | 12 | 10 | 12 | ns | 30 |

| AC Characteristics - Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Clock cycle time CL = 3 | tCK | 5 | 7.5 | 5 | 7.5 | 5 | 7.5 | ns | 30 |
| Clock cycle time CL = 2.5 | tCK | 5 | 12 | 6 | 12 | 6 | 12 | ns | 30 |
| Clock cycle time CL = 2 | tCK | 7.5 | 12 | 7.5 | 12 | 10 | 12 | ns | 30 |

**Table 38** AC Timing Variations for DDR 333, DDR 266 & DDR 200 Devices

| | DDR 333B | | DDR 266A | | DDR 266B | | DDR 200 | | DDR 200B | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| tCK CL = 2.5 | 6 | 12 | 7.5 | 12 | 7.5 | 12 | 10 | 12 | 10 | 12 | ns |
| tCK CL = 2.0 | 7.5 | 12 | 7.5 | 12 | 10 | 12 | 10 | 12 | 10 | 12 | ns |

NOTE 30: The only time that the clock frequency is allowed to change is during self-refresh mode.

## PASS Condition

The tCK(avg) measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79E*.

## Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures a sliding “window” of 200 cycles.
2. Calculate the average period value for periods 1-200, 2-201 and 3-202.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

## Test References

See Table 11 - Electrical Characteristics and AC Timing and Table 12 - AC Timing Variations for DDR 333, DDR 266 and DDR 200 Devices, in the *JEDEC Standard JESD79E*.

# Average High Pulse Width - tCH(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

## Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

## Test Definition Notes from the Specification.

**Table 39** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |

## Pass Condition

The tCH measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79E*.

## Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding "window" of 200 cycles.
2. Measure the width of the high pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).

4 Compare the test results against the compliance test limits.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# Average Low Pulse Width - tCL(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

## Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

## Test Definition Notes from the Specification.

**Table 40** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |

## Pass Condition

The tCL measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79E*.

## Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding "window" of 200 cycles.
2. Measure the width of the low pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).

4 Compare results against the compliance test limits.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# 8 Data Strobe Timing (DST) Tests



This section provides the Methods of Implementation (MOIs) for Data Strobe Timing tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

**NOTE** Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

# Probing for Data Strobe Timing Tests

When performing the Data Strobe Timing tests, the DDR1 Compliance Test Application will prompt you to make the proper connections. The connection for Data Strobe Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR1 Compliance Test Application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

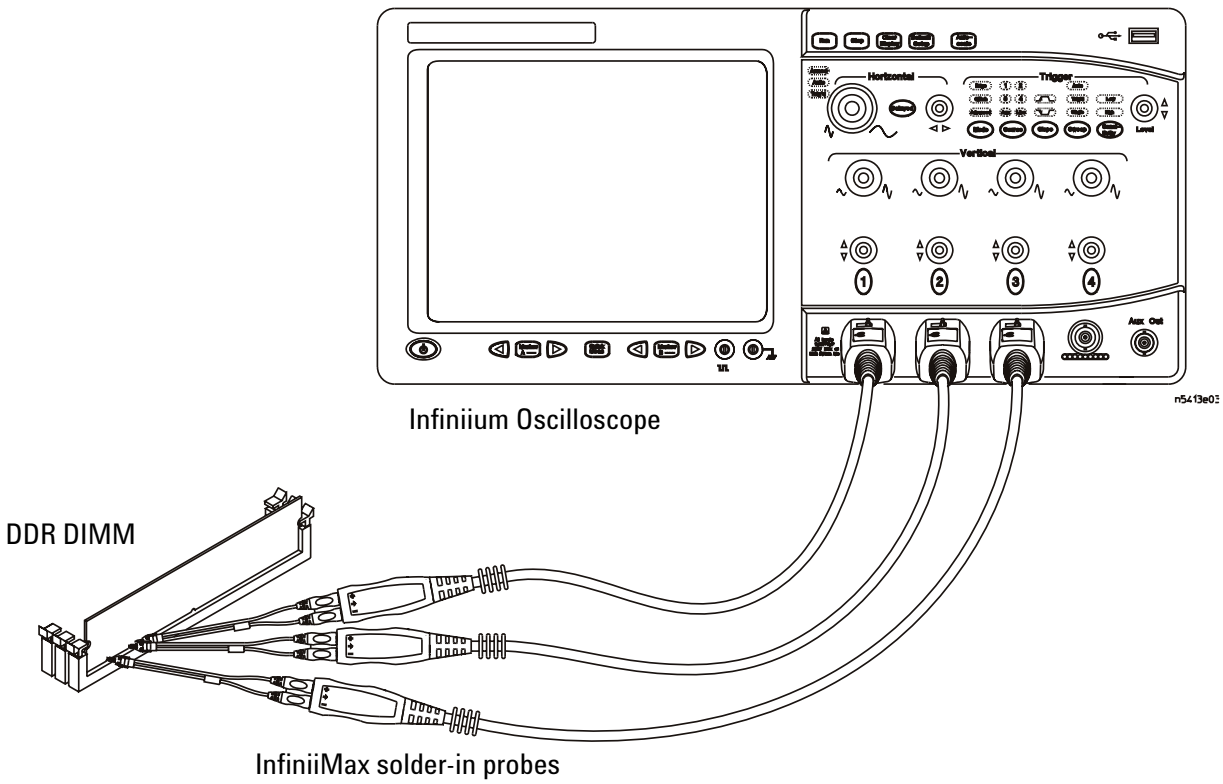


**Figure 33** Probing for Data Strobe Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channels shown in Figure 33 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1. Start the automated test application as described in “Starting the DDR1 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR1 Test Application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR1-200, DDR1-266, DDR1-333, DDR1-400.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

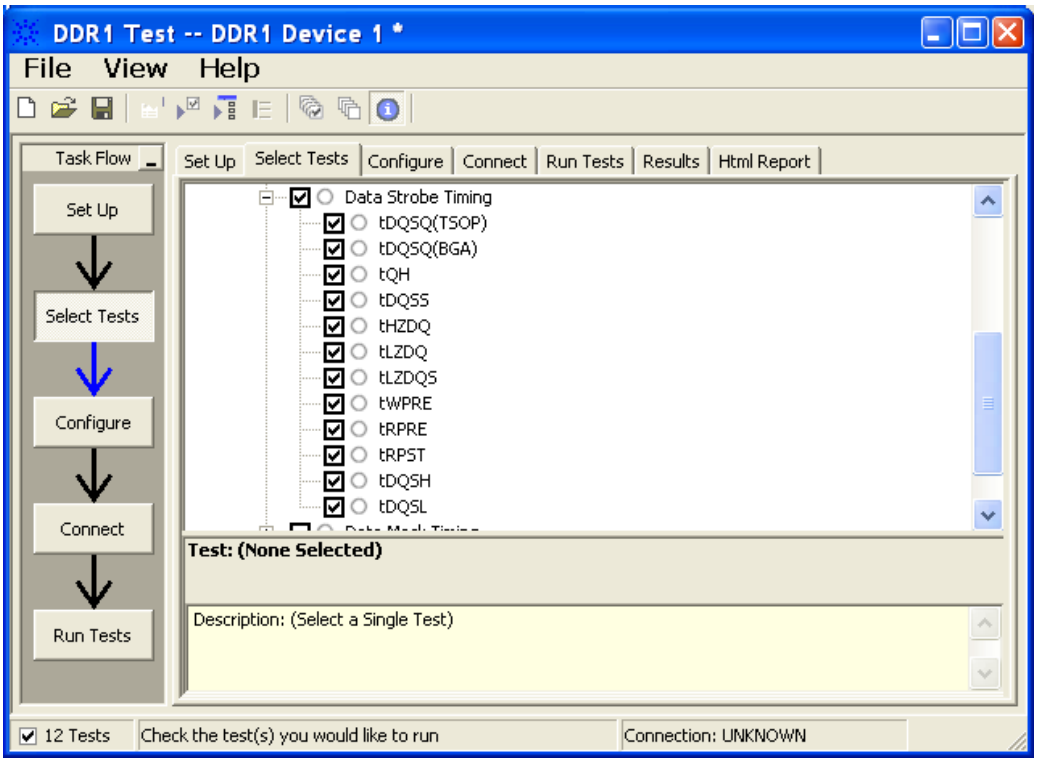


**Figure 34** Selecting Data Strobe Timing Tests

**9** Follow the DDR1 Test application's task flow to set up the configuration options (see Table 41), run the tests and view the tests results.

**Table 41** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **Timing Tests** | |
| Total Bit Display | Allows user to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals. |
| Verify Selected Rank Only? | If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope. |
| Channel (1,2,3) | Signal connected to the specific channel. |
| Pin Under Test, PUT | Signal used for testing. |

# tHZ(DQ), DQ High Impedance Time From CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ is no longer driving (from high state OR low state to the high impedance stage), to the clock signal crossing, is within the conformance limits as specified in the *JEDEC Standard JESD79E*.

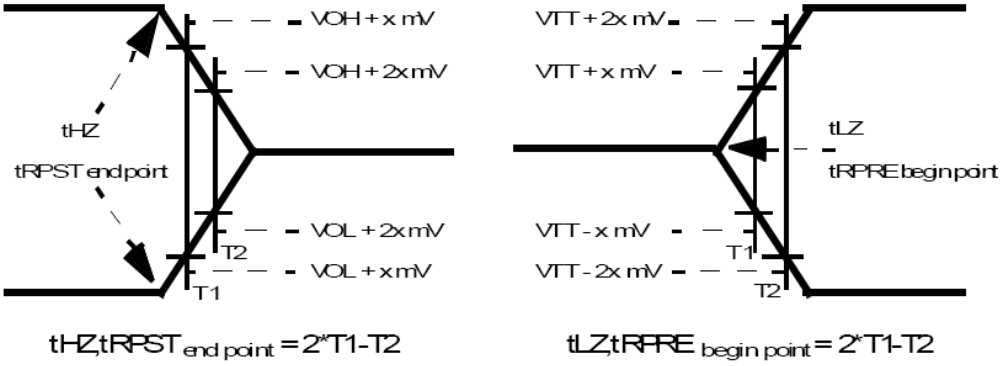


**Figure 35** Method for Calculating Transitions and Endpoints

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 42** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS high-impedance time from CK/$\overline{CK}$ | tHZ | | +0.7 | | +0.7 | | +0.7 | ns | 15 |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS high-impedance time from CK/$\overline{CK}$ | tHZ | | +0.7 | | +0.7 | | +0.7 | ns | 15 |

NOTE 15: tHZ and tLZ transitions occurs in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begin driving (tLZ). Figure 35 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

## PASS Condition

The measured time interval from the point where the DQ starts to transit from high/low state to high impedance state, to the clock signal crossing point should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the right from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function, using Clock as the reference to define the Histogram Window for the DQ signal.

10 The Histogram Window is required to cover the DQ signal from the high/low state to the moment it starts to turn off the driver into tristate.

11 Setup the threshold value and measurement point for the DQ signal based on the histogram result.

12 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQ starts to transit from high/low to the time when it turned off its driver into tristate.

13 Assign marker A for the clock signal crossing point while marker B for the data signal start to turn off its driver.

14 Measure delta of marker A and marker B and this will be the test result.

15 Compare the test result against the compliance test limit.

**NOTE** Some designs do not have tristate at $V_{REF}$ (for example, 0.9V). This test is not guaranteed when this scenario happens, as there is no significant point of where the driver has been turned-off.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tHZ(DQS), DQS High Impedance Time From CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts driving (from tristate to high state OR low state stage), to the clock signal crossing, is within the conformance limits as specified in the *JEDEC Standard JESD79E*.

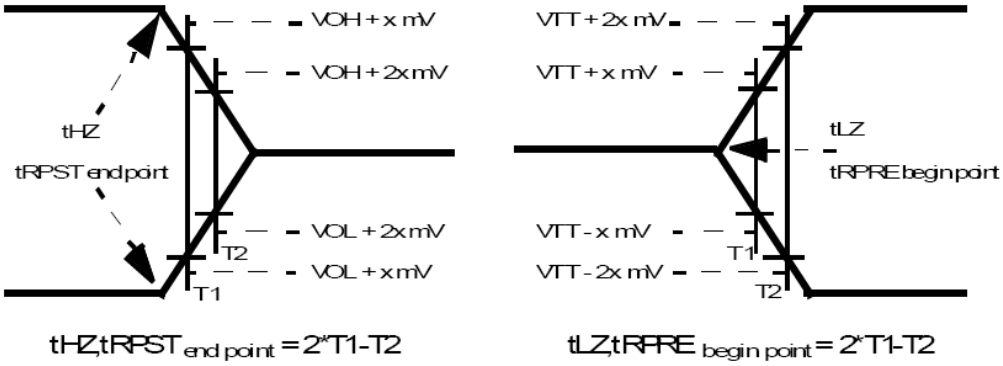


**Figure 36** Method for Calculating Transitions and Endpoints

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 43** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS high-impedance time from CK/$\overline{CK}$ | tHZ | | +0.7 | | +0.7 | | +0.7 | ns | 15 |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS high-impedance time from CK/$\overline{CK}$ | tHZ | | +0.7 | | +0.7 | | +0.7 | ns | 15 |

NOTE 15: tHZ and tLZ transitions occurs in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begin driving (tLZ). Figure 36 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

## PASS Condition

The measured time interval from the point where the DQS starts to transit from tristate to the moment it starts to drive at high/low state, to the clock signal crossing point should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the right from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function, using Clock as the reference to define the Histogram Window for the DQS signal.

10 The Histogram Window is required to cover the DQS signal from the high/low state to the moment it starts to turn off the driver into tristate.

11 Setup the threshold value and measurement point for the DQS signal based on the histogram result.

12 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from high/low to the time when it turned off its driver into tristate.

13 Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.

14 Measure delta of marker A and marker B and this will be the test result.

15 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tLZ(DQS), DQS Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts driving (from tristate to high/low state) to the clock signal crossing, is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

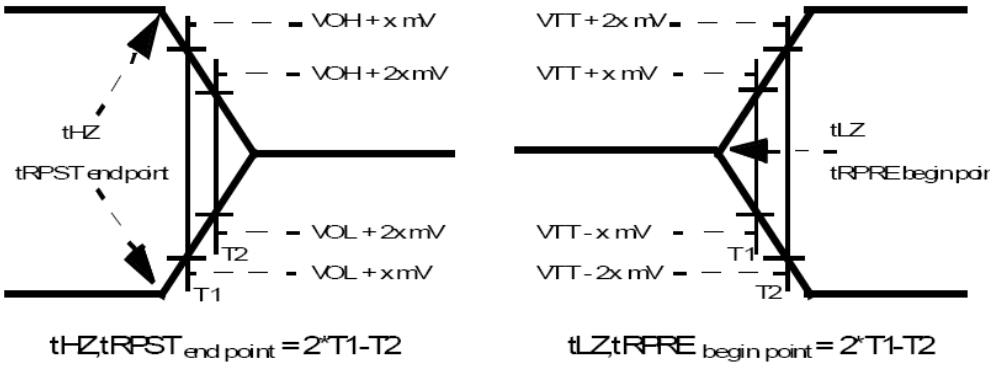


**Figure 37** Method for Calculating Transitions and Endpoints

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 44** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS high-impedance time from CK/$\overline{CK}$ | tHZ | | +0.7 | | +0.7 | | +0.7 | ns | 15 |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS high-impedance time from CK/$\overline{CK}$ | tHZ | | +0.7 | | +0.7 | | +0.7 | ns | 15 |

NOTE 15: tHZ and tLZ transitions occurs in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begin driving (tLZ). Figure 37 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

## PASS Condition

The measured time interval from the point where the DQS starts to transit from tristate to the moment when it starts to drive high/low (high impedance state to high/low state) to the clock signal crossing point, should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It

uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function, using the Clock as the reference to define the Histogram Window for the DQS signal.

10 The Histogram Window is required to cover the DQS signal from tristate to the moment it starts to drive the signal high/low.

11 Setup the threshold value and measurement point for the DQS signal based on the histogram result.

12 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it start to drive high/low.

13 Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.

14 Measure delta of marker A and marker B and this will be the test result.

15 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

## tLZ(DQ), DQ Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to high/low state), to the clock signal crossing, is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

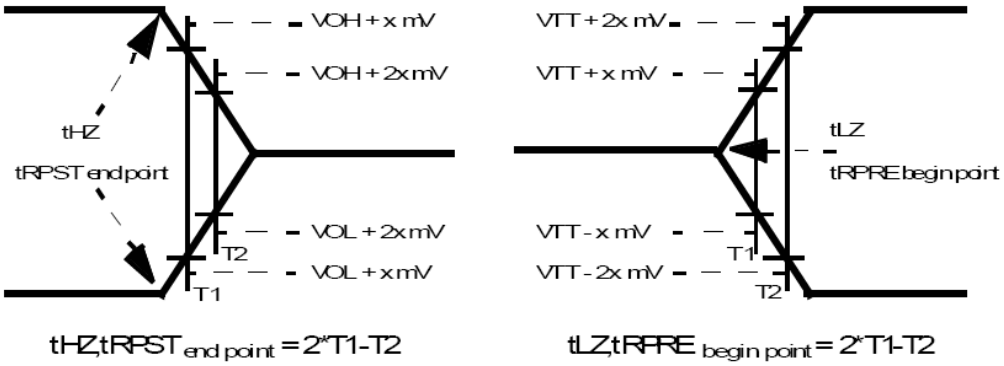


**Figure 38** Method for Calculating Transitions and Endpoints

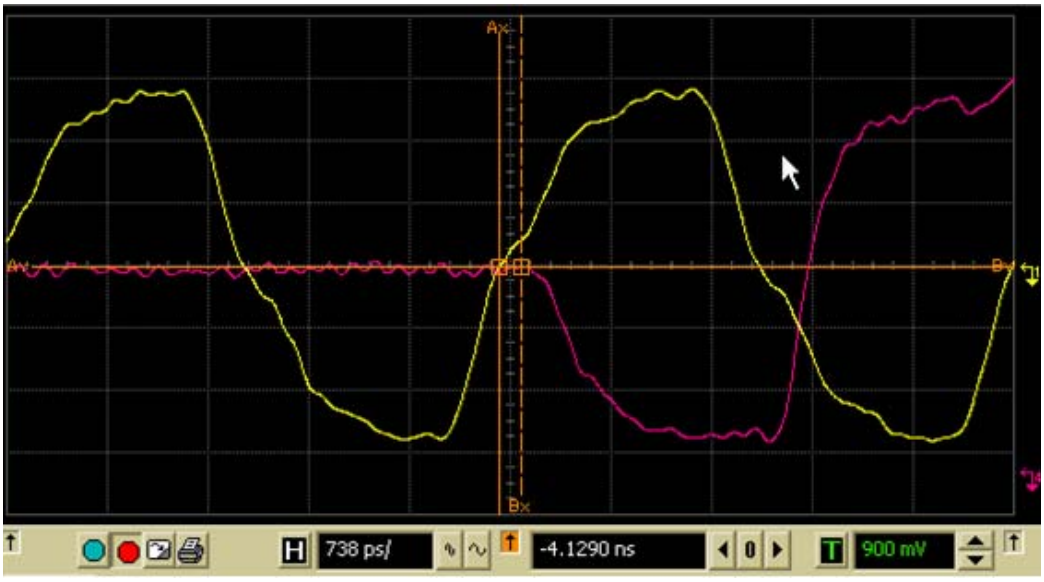


**Figure 39** tLZ(DQ) in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 45** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS low-impedance time from CK/$\overline{CK}$ | tLZ | -0.70 | +0.70 | -0.75 | +0.75 | -0.8 | +0.8 | ns | 15 |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS low-impedance time from CK/$\overline{CK}$ | tLZ | -0.70 | +0.70 | -0.70 | +0.70 | -0.70 | +0.70 | ns | 15 |

NOTE 15: tHZ and tLZ transitions occurs in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begin driving (tLZ). Figure 38 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

## PASS Condition

The measured time interval from the point where the DQ starts to transit from high impedance to the moment when it starts to drive high/low (high impedance state to high/low state), to the clock signal crossing point, should be within the specification limit.

## Measurement Algorithm

1 Obtain the parameters and settings from the Configuration page.

2 Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the "BinaryEdgeNormal" function, using the Clock as the reference to define the Histogram Window for the DQ signal.

10 The Histogram Window is required to cover the DQ signal from the tristate to the moment it starts to drive high/low state.

11 Setup the threshold value and measurement point for the DQ signal based on the histogram result.

12 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQ starts to transit from tristate to the time when it start to drive the signal high/low.

13 Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.

14 Measure delta of marker A and marker B and this will be the test result.

15 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 46** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| DQS-DQ Skew (for DQS & associated DQ signals) | TSOP Pkg | tDQSQ | | +0.45 | | +0.5 | | +0.6 | ns | 26 |
| | BGA Pkg | tDQSQ | | +0.4 | | +0.5 | | +0.6 | ns | 26 |

| AC Characteristics Parameter | | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| DQS-DQ Skew (for DQS & associated DQ signals) | TSOP Pkg | tDQSQ | | +0.4 | | +0.4 | | +0.4 | ns | 26 |
| | BGA Pkg | tDQSQ | | +0.4 | | +0.4 | | +0.4 | ns | 26 |

NOTE 26: tDQSQ Consists of data pin skew and output pattern effects, and p=channel to n-channel variation of the output drivers for any given cycle.

## PASS Condition

The measured time interval between the data strobe and the associated data signal should be within specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read Cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the "BinaryEdgeNormal" function to obtain the Edge number of the DQS and DQ signal. This Edge number will be used for the TEdge measurement, in order to locate the points of interest on specific signal.
10. After obtaining the Edge number for the respective signal, begin the tDQSQ measurement bit by bit in the Read data burst, beginning from the 1st bit of the Read cycle.
11. Begin at the 1st bit of the Read cycle, from the Read preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).
12. DQS-Clock timing measurement compares the rising edge (Vih_ac OR Vil_dc against DQS crossing) OR the falling edge (Vih_ac OR Vil_dc against DQS crossing).
13. Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tQH, DQ/DQS Output Hold Time From DQS - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data output hold time (DQ rising and falling edge) from the DQS (rising and falling edge) is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 47** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS output hold time from DQS | tQH | tQP-tQHS | | tQP-tQHS | | tQP-tQHS | | ns | 25 |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DQS output hold time from DQS | tQH | tQP-tQHS | | tQP-tQHS | | tQP-tQHS | | ns | 25 |

NOTE 25: tQH = tHP - tQHS, where:

tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits; and

2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

## PASS Condition

The measured time interval between the data output hold time and the associated data strobe signal should be within specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the DQS and DQ signal. This Edge number will be used for the TEdge measurement, in order to locate the points of interest on specific signal.
10. After obtaining the Edge number for the respective signal, begin the tQH measurement bit by bit in Read Data Burst, beginning from the 1st bit of the Read cycle.
11. Begin at the 1st bit of the Read cycle, from the Read preamble. Continue the measurement until the last bit (for instance, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).
12. DQS-DQ timing measurement compares the rising edge (DQS crossing against Vil_dc of the DQ signal, for instance, end of valid DQ hold time)

OR the falling edge (DQS crossing against Vih_dc of the DQ signal, for instance, end of valid DQ hold time).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the lock signal while marker B for the data signal, for the Worst Case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tDQSS, DQS Latching Transition to Associated Clock Edge - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS falling edge) access time to the associated clock (crossing point) is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

## Test Definition Notes from the Specification

**Table 48** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Write command to first DQS latching transition | tDQSS | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | tCK | |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Write command to first DQS latching transition | tDQSS | 0.72 | 1.25 | 0.72 | 1.25 | 0.72 | 1.25 | tCK | |

## PASS Condition

The measured time interval between the rising edge of the data strobe access output and the clock crossing should be within specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of clock rising edge and strobe rising edge. This Edge number will be used for TEdge measurement, in order to locate the points of interest on specific signal.
10. After obtaining the Edge number for the respective signal, begin the tDQSS measurement bit by bit in the Write data burst, beginning from the 1st bit of the Write cycle. Begin at the 1st bit of the read cycle, from the Write preamble.
11. Continue the measurement until the last bit (for instance, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).
12. DQS-Clock timing measurement compares the rising edge (DQS crossing against clock crossing) OR the falling edge (DQS crossing against Vih_dc of the DQ signal, for instance, end of valid DQ hold time).
13. Within the data burst, measure each bit, for instance the rising edge of the DQS-Clock. Capture the worst case data each time a new value is measured.
14. Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.
15. Measure delta of marker A and marker B and this will be the test result.
16. Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tDQSH, DQS Input High Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high level of the data strobe signal is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

## Test Definition Notes from the Specification

**Table 49** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS input high pulse width | tDQSH | 0.35 | | 0.35 | | 0.35 | | tCK | |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS input high pulse width | tDQSH | 0.35 | | 0.35 | | 0.35 | | tCK | |

## PASS Condition

The measured pwidth of the data strobe signal should be within specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
4. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
5. If you have selected the $\overline{CS}$ option, skip the next step and go to step 7.
6. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The for loops, TEdge and Delta Time are used to search the preamble.
7. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.
8. After obtaining the Edge number for the respective signal, begin the tDQSH measurement by using the Pwidth function to find any rising edge of the data strobe signal and measure the pwidth for every single bit in the captured data burst.
9. Assign marker A for the rising edge of the clock signal while marker B for the falling edge of the clock signal.
10. Measure delta of marker A and marker B and this will be the test result.
11. Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tDQSL, DQS Input Low Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the low level of the clock signal is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 50** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS input low pulse width | tDQSL | 0.35 | | 0.35 | | 0.35 | | tCK | |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS input low pulse width | tDQSL | 0.35 | | 0.35 | | 0.35 | | tCK | |

## PASS Condition

The measured nwidth of the clock signal should be within specification limit.

## Measurement Algorithm

1 Obtain the parameters and settings from the Configuration page.

2 Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The for loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the "BinaryEdgeNormal" function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSL measurement by using the Nwidth function to find any rising edge of the data strobe signal and measure the nwidth for every single bit in the captured data burst.

11 Assign marker A for the rising edge of the clock signal while marker B for the falling edge of the clock signal.

12 Measure delta of marker A and marker B and this will be the test result.

13 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tDSS, DQS Falling Edge to CK Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock setup time, is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 51** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS falling edge to CK setup time | tDSS | 0.2 | | 0.2 | | 0.2 | | tCK | |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS falling edge to CK setup time | tDSS | 0.2 | | 0.2 | | 0.2 | | tCK | |

## PASS Condition

The measured time interval between the falling edge of the data strobe access output to the associated clock setup time should be within the specification limit.

## Measurement Algorithm

1 Obtain the parameters and settings from the Configuration page.

2 Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the "BinaryEdgeNormal" function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDSS measurement bit by bit in Write data burst.

11 Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 DQS-Clock timing measurement compares the rising edge (DQS falling against clock crossing).

13 DQ-Clock timing measurement compares the falling edge of the DQS to the clock setup time. The worst case data will be captured each time new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tDSH, DQS Falling Edge Hold Time from CK - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe output access time to the hold time of the clock, must be within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 52** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS falling edge hold time from CK | tDSH | 0.2 | | 0.2 | | 0.2 | | tCK | |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS falling edge hold time from CK | tDSH | 0.2 | | 0.2 | | 0.2 | | tCK | |

## PASS Condition

The measured time interval between the falling edge of the data strobe hold time from the associated clock crossing edge should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.
10. After obtaining the Edge number for the respective signal, begin the tDSH measurement bit by bit in Write data burst.
11. Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).
12. DQS-Clock timing measurement compares the falling edge of the DQS crossing hold time from the respective clock crossing edge.
13. Within the data burst, each bit, for instance, the falling edge of DQS-Clock will be measured. The worst case data will be captured each time a new value is measured.
14. Once all the bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.
15. Measure delta of marker A and marker B and this will be the test result.
16. Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tWPST, Write Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high impedance) from the last DQS signal crossing (last bit of the write data burst) for the Write cycle, is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 53** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Write postamble | tWPST | 0.40 | 0.60 | 0.40 | 0.60 | 0.40 | 0.60 | tCK | 16 |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Write postamble | tWPST | 0.40 | 0.60 | 0.40 | 0.60 | 0.40 | 0.60 | tCK | 16 |

NOTE 16: The maximum limit for this parameter is not device limit. The device will operate with greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

## PASS Condition

The measured time interval between the last DQS signal crossing point and the point where the DQS starts to transit from high/low state to high impedance should be within the specification limit.

## Measurement Algorithm

1 Obtain the parameters and settings from the Configuration page.

2 Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS postamble towards the right from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the postamble.

9 Once the postamble is located, call the “BinarySearchNormal” function to locate the last DQS crossing point or reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS postamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from high/low to the time when it starts to turn off the driver low (for instance, end of burst or postamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to turn off driver.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tWPRE, Write Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts to drive low (preamble behavior) to the first DQS signal crossing for the Write cycle, is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

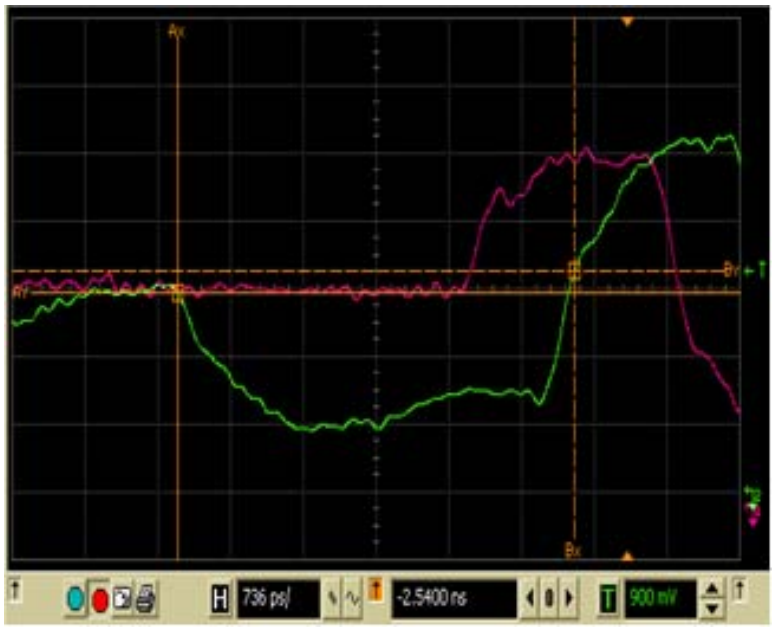


**Figure 40** tWPRE in Infiniium oscilloscope

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{\text{CS}}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 54** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Write preamble | tWPRE | 0.25 | | 0.25 | | 0.25 | | tCK |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Write preamble | tWPRE | max (0.25*tCK, 1.5 ns) | | max (0.25*tCK, 1.5 ns) | | max (0.25*tCK, 1.5 ns) | | ns |

## PASS Condition

The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Write cycle, should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinarySearchNormal” function to locate the first DQS crossing point or the reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS preamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it starts to drive low (for instance, beginning of preamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to drive low.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tRPRE, Read Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS start driving low (*preamble behavior) to the first DQS signal crossing for the Read cycle must be within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{\text{CS}}$ as additional signal, which requires additional channel)

## Test Definition Notes from the Specification

**Table 55** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| Read preamble | CL = 2.5 | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | 28, 33 |
| | CL = 2.0 | | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | 28, 33 |
| | CL = 2.5 | | NA | NA | NA | NA | - | 1.1 | tCK | 28, 33 |

| AC Characteristics Parameter | | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| Read preamble | CL = 3 | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | 28, 33 |
| | CL = 2.5 | | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | 28, 33 |
| | CL = 2.0 | | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | 28, 33 |
| | CL = 1.5 | | NA | NA | NA | NA | NA | NA | | |

NOTE 28: Optional CAS Latency, 1.5, is only defined for DDR 200 speed grade

NOTE 33: tRPST end; point adn tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE).

## PASS Condition

The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Read cycle should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinarySearchNormal” function to locate the first DQS crossing point or the reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS preamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it start to drive low (for instance, beginning of preamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to drive low.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tRPST, Read Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high-impedance) to the last DQS signal crossing (last bit of the data burst) for the Read cycle is within the conformance limit as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 56** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 33 |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 33 |

NOTE 33: tRPST end; point adn tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE).

## PASS Condition

The measured time interval between the last DQS signal crossing point to the point where the DQS starts to transit from high/low level to high impedance for the Read cycle should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope setting. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS postamble towards the right from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the postamble.
9. Once the postamble is located, call the “BinarySearchNormal” function to locate the last DQS crossing point or reference point.
10. Define the histogram window in order to obtain the Min and Max voltage for the DQS postamble signal and it will be used for the threshold setup for the trigonometry calculation later.
11. Once all points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from high/low to the time when it starts to turn off the driver low (for instance, end of burst, postamble).
12. Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to turn off the driver.
13. Measure delta of marker A and marker B and this will be the test result.
14. Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# 9 Data Mask Timing (DMT) Tests



This section provides the Methods of Implementation (MOIs) for Data Mask Timing tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

**NOTE** Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

# Probing for Data Mask Timing Tests

When performing the Data Mask Timing tests, the DDR1 Compliance Test Application will prompt you to make the proper connections. The connection for Data Mask Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR1 Compliance Test Application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

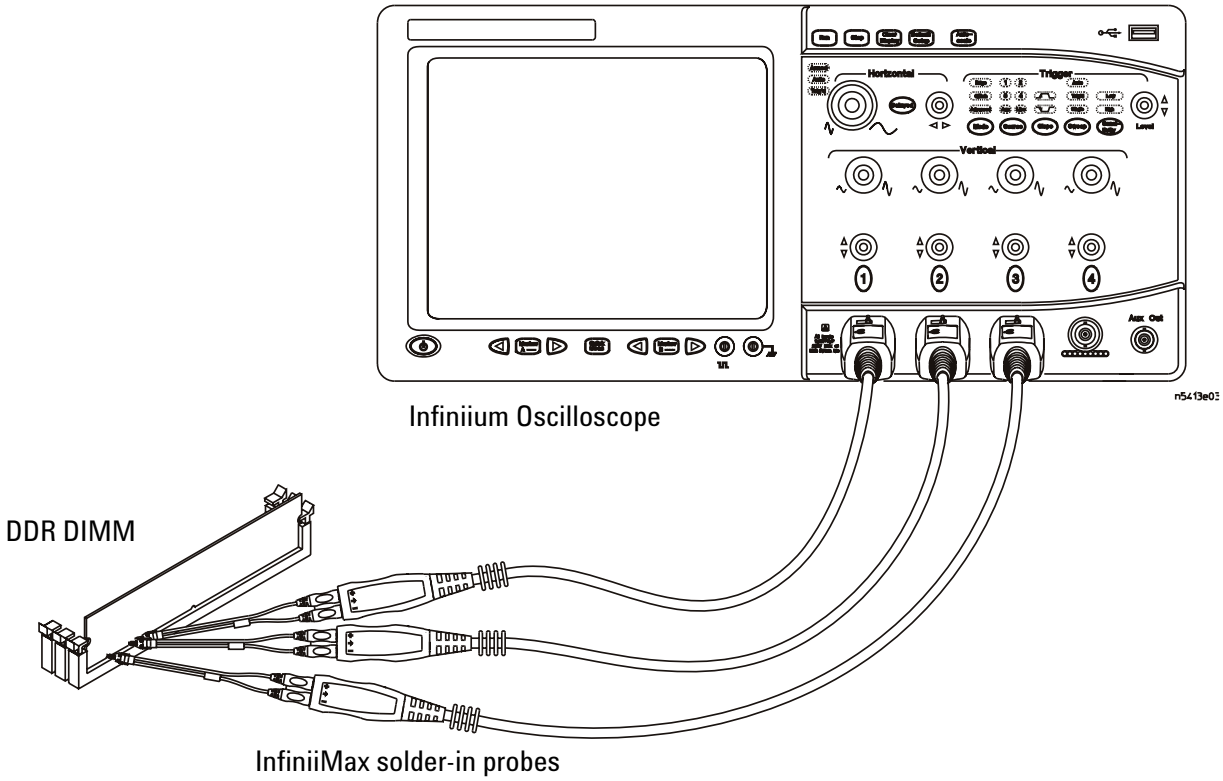


**Figure 41** Probing for Data Mask Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channels shown in Figure 41 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1. Start the automated test application as described in “Starting the DDR1 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR1 Test Application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR1-200, DDR1-266, DDR1-333, DDR1-400.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

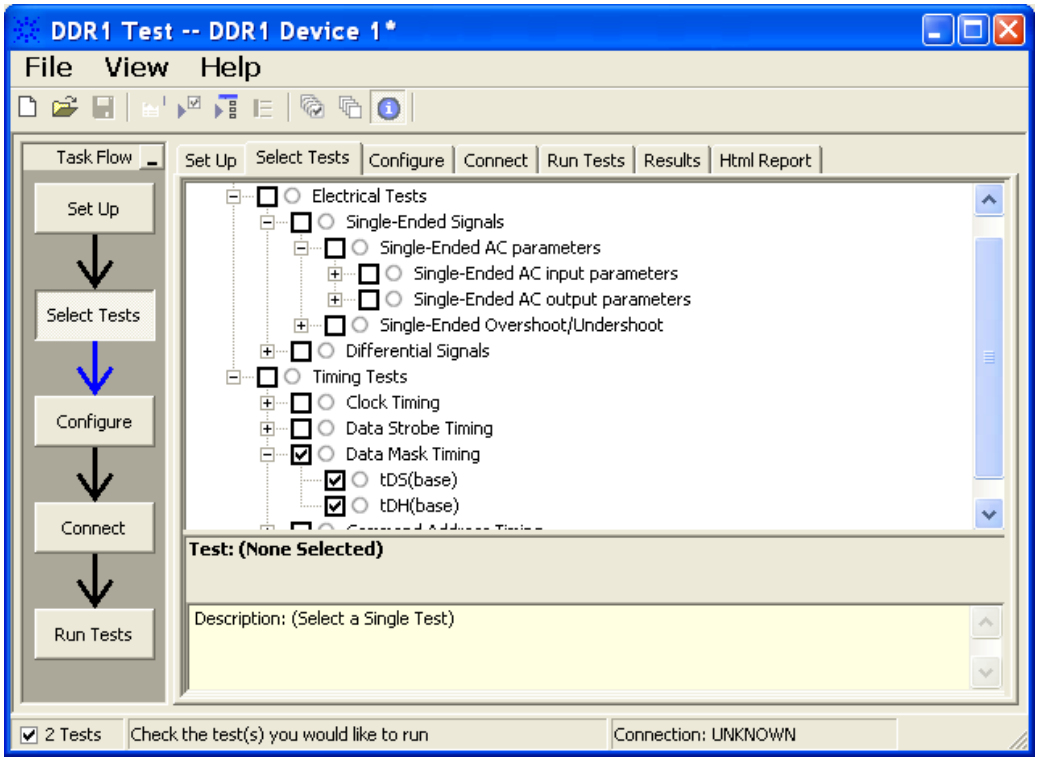


**Figure 42** Selecting Data Mask Timing Tests

**9** Follow the DDR1 Test Application's task flow to set up the configuration options (see Table 57), run the tests and view the tests results.

**Table 57** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **Timing Tests** | |
| Total Bit Display | Allows user to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals. |
| Verify Selected Rank Only? | If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope. |
| Channel (1,2,3) | Signal connected to the specific channel. |
| Pin Under Test, PUT | Signal used for testing. |

# tDS(base), DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling Edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (DQ as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

## Test Definition Notes from the Specification

**Table 58** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DM input setup time | tDS | 0.45 | | 0.5 | | 0.6 | | ns | 31, j, k |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DM input setup time | tDS | 0.4 | | 0.4 | | 0.4 | | ns | 31 |

NOTE j: A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

The delta rise/fall rate is calculated as:

{1/(Slew Rate1)}-{1/(Slew Rate2)}

NOTE k: The 1/0 slew rate is based on the lesser of the AC-AC slew rate and the DC-DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(A) or VIH(DC) to VIH(DC), and similarly for rising transitions. A derating factor applies to speed bins DDR 200, DDR 266, and DDR 333.

NOTE 31: If refreshing timing or tDS/tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

## PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS crossing point should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the rise/fall DQS crossing and Vih_ac/Vil_ac DQ for later TEdge measurement use. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDS(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble.

11 Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 The DQS-DQ timing measurement compares the rising edge (DQ rising, for instance Vih_ac against associated DQS crossing) OR the falling edge (DQ falling, for instance Vil_ac against associated DQS crossing).

13 Within the data burst, measure each bit, for instance rising and falling edge of DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# tDH(base), DQ and DM Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

## Test Definition Notes from the Specification

**Table 59** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DM input hold time | tDH | 0.45 | | 0.5 | | 0.6 | | ns | 31, j, k |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DM input hold time | tDH | 0.4 | | 0.4 | | 0.4 | | ns | 31 |

NOTE j: A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

The delta rise/fall rate is calculated as:

{1/(Slew Rate1)}-{1/(Slew Rate2)}

NOTE k: The 1/0 slew rate is based on the lesser of the AC-AC slew rate and the DC-DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(A) or VIH(DC) to VIH(DC), and similarly for rising transitions. A derating factor applies to speed bins DDR 200, DDR 266, and DDR 333.

NOTE 31: If refreshing timing or tDS/tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

## PASS Condition

The measured time interval between the data or data mask (DQ/DM) hold time to the respective DQS crossing point should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the rise/fall DQS crossing and the Vih_dc/Vil_dc DQ for the later TEdge measurement use. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDH(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble.

11 Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 The DQS-DQ timing measurement compares the rising edge (DQ rising, for instance Vil_dc against associated DQS crossing) OR the falling edge (DQ falling, for instance Vih_dc against associated DQS crossing).

13 Within the data burst, measure each bit, for instance rising and falling edge of the DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical Characteristics and AC Timing, in the *JEDEC Standard JESD79E*.

# 10 Command and Address Timing (CAT) Tests



This section provides the Methods of Implementation (MOIs) for Command and Address Timing tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

**NOTE** Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

# Probing for Command and Address Timing Tests

When performing the Command and Address Timing tests, the DDR1 Compliance Test Application will prompt you to make the proper connections. The connection for Command and Address Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR1 Compliance Test Application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

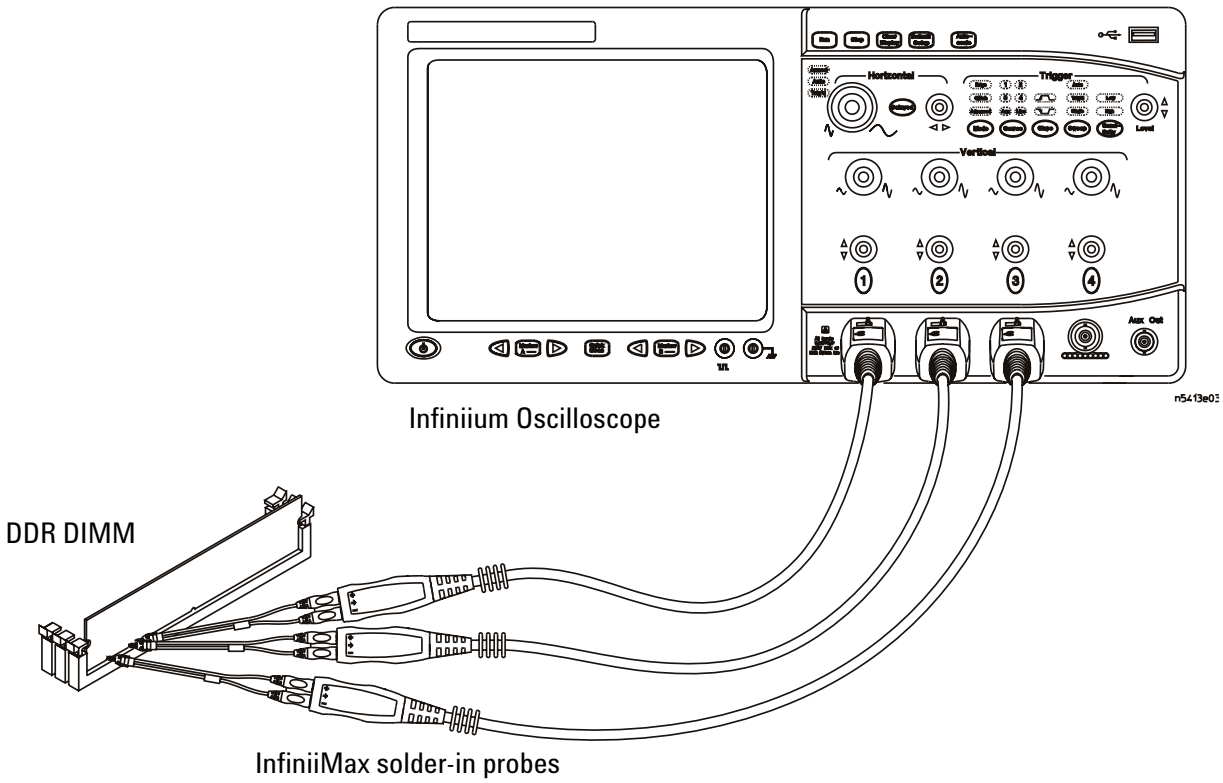


**Figure 43** Probing for Command and Address Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channels shown in Figure 43 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1. Start the automated test application as described in “Starting the DDR1 Compliance Test Application" on page 25.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR1 Test Application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR1-200, DDR1-266, DDR1-333, DDR1-400.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

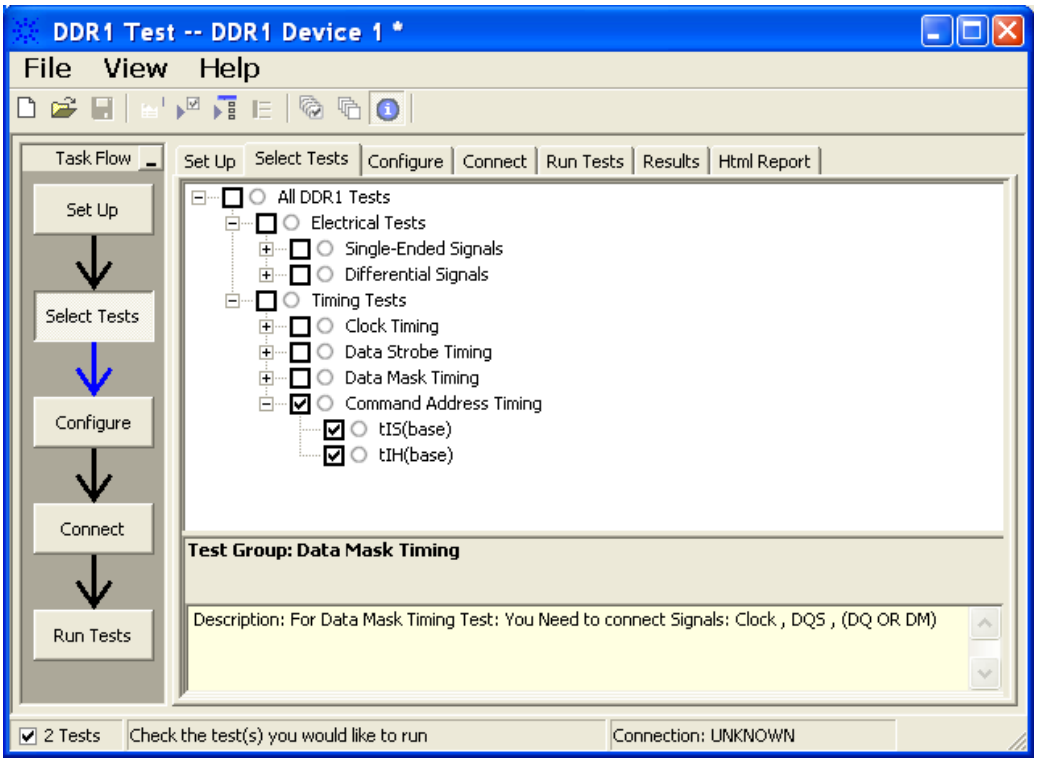


**Figure 44** Selecting Command and Address Timing Tests

**9** Follow the DDR1 Test application's task flow to set up the configuration options (see Table 60), run the tests and view the tests results.

**Table 60** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **Timing Tests** | |
| Total Bit Display | Allows user to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals. |
| Total Measurement Required | To perform the total number of measurement based on user selection. |
| Option | Identifies the signal used for testing. |
| Pin Under Test, PUT | Signal used for testing. |

# tIS(base) - Address and Control Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits of the $V_{ID(ac)}$ as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Read cycle only):

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

## Test Definition Notes from the Specification

**Table 61** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Address and Control input setup time (fast slew rate) | tIS | 0.75 | | 0.9 | | 1.1 | | ns | 19, 21-23, i |
| Address and Control input setup time (slow slew rate) | tIS | 0.80 | | 1.0 | | 1.1 | | ns | 20-23, j |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Address and Control input setup time (fast slew rate) | tIS | 0.60 | | 0.60 | | 0.60 | | ns | 19, 21-23 |
| Address and Control input setup time (slow slew rate) | tIS | 0.70 | | 0.70 | | 0.70 | | ns | 20-23 |

NOTE i: A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns. The input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. A derating factor applies to speed bins DDR 200, DDR 266 and DDR 333.

NOTE 19: For command/address input slew rate ≥ 1.0 V/ns.

NOTE 20: For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns.

NOTE 21: For CK and CK#, slew rate ≥ 1.0 V/ns (single-ended).

NOTE 22: These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

NOTE 23: Slew Rate is measured between VOH(AC) and VOL(AC).

## PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the CK-DQS.
5. tIS measurement will compare the rising edge (address/control rising e.g. Vih_ac against associated clock crossing) OR falling edge (address/control falling e.g. Vil_ac against associated clock crossing).
6. Assign marker A for the clock signal while marker B for the data signal, for the final measurement result.
7. Measure delta of marker A and marker B and this will be the test result.
8. Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical and AC Timing, in the *JEDEC Standard JESD79E*.

# tIH(base) - Address and Control Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79E*.

## Signals of Interest

Based on the test definition (Read cycle only):

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

## Test Definition Notes from the Specification

**Table 62** Electrical Characteristics and AC Timing

| AC Characteristics Parameter | Symbol | DDR 333 | | DDR 266 | | DDR 200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Address and Control input hold time (fast slew rate) | tIH | 0.75 | | 0.9 | | 1.1 | | ns | 19, 21-23, i |
| Address and Control input hold time (slow slew rate) | tIH | 0.80 | | 1.0 | | 1.1 | | ns | 20-23, j |

| AC Characteristics Parameter | Symbol | DDR 400A (2.5-3-3) | | DDR 400B (3-3-3) | | DDR 400C (3-4-4) | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Address and Control input setup time (fast slew rate) | tIH | 0.60 | | 0.60 | | 0.60 | | ns | 19, 21-23 |
| Address and Control input setup time (slow slew rate) | tIH | 0.70 | | 0.70 | | 0.70 | | ns | 20-23 |

NOTE i: A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns. The input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. A derating factor applies to speed bins DDR 200, DDR 266 and DDR 333.

NOTE 19: For command/address input slew rate ≥ 1.0 V/ns.

NOTE 20: For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns.

NOTE 21: For CK and CK#, slew rate ≥ 1.0 V/ns (single-ended).

NOTE 22: These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

NOTE 23: Slew Rate is measured between VOH(AC) and VOL(AC).

## PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

## Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the CK-DQS.
5. tIH measurement will compare the rising edge (address/control rising e.g. Vih_dc against associated clock crossing) OR falling edge (address/control falling e.g. Vil_dc against associated clock crossing).
6. Assign marker A for the clock signal while marker B for the data signal, for the final measurement result.
7. Measure delta of marker A and marker B and this will be the test result.
8. Compare the test result against the compliance test limit.

## Test References

See Table 11 - Electrical and AC Timing, in the *JEDEC Standard JESD79E*.

# 11 Advanced Debug Mode Clock Tests



This section provides the Methods of Implementation (MOIs) for Rising Edge and Pulse Measurements Clock tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

## Probing for Clock Tests

When performing the Advanced Debug Mode Clock tests, the DDR1 Compliance Test Application will prompt you to make the proper connections. The connections for Rising Edge and Pulse Measurement Clock tests may look similar to the following diagram. Refer to the Connection tab in DDR1 Electrical Performance Compliance application for the exact number of probe connections.

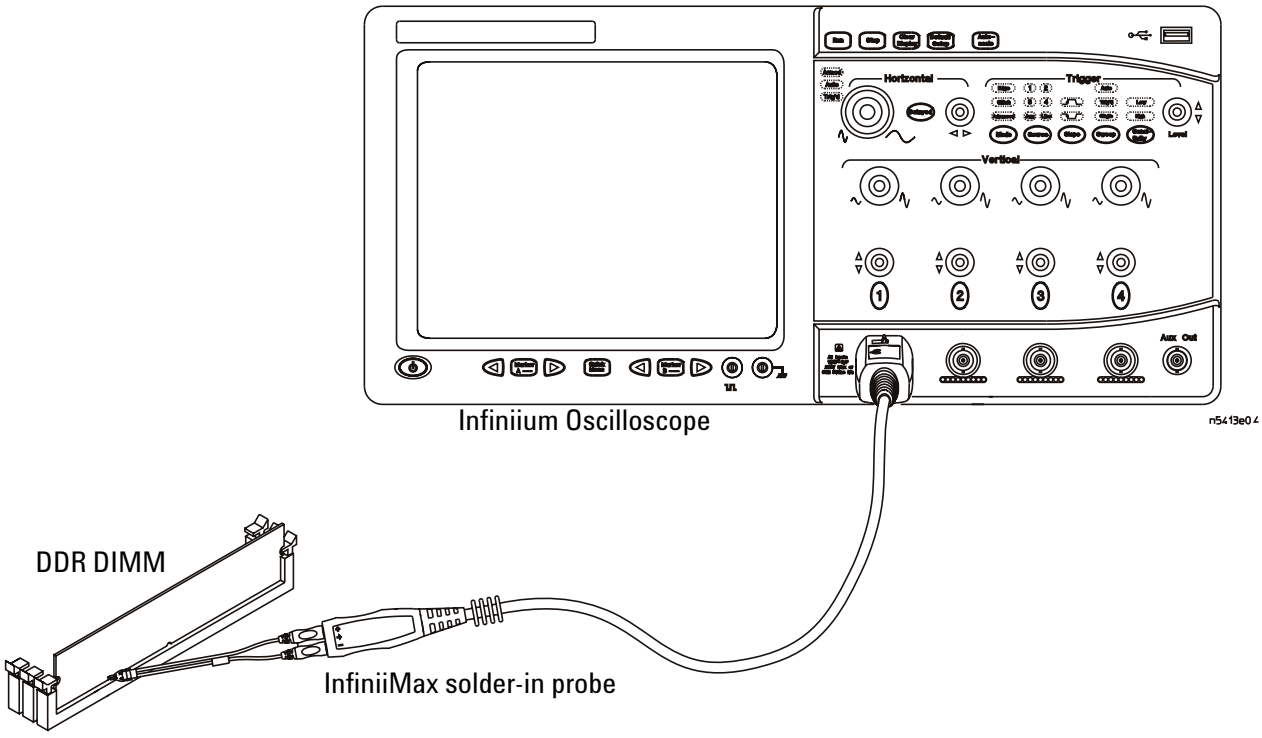


**Figure 45** Probing for Measurement Clock Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channel shown in Figure 45 is just an example.)

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1 Start the automated test application as described in "Starting the DDR1 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR Device Under Test (DUT) is attached. This software will perform tests on all the unused RAM in the system by producing repetitive bursts of read-write data signals to the DDR memory.

3 Connect the differential solder-in probe head to the PUT on the DDR DIMM.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR1 test application, click the Set Up tab.

6 Select Advanced Debug as the Test Mode option.

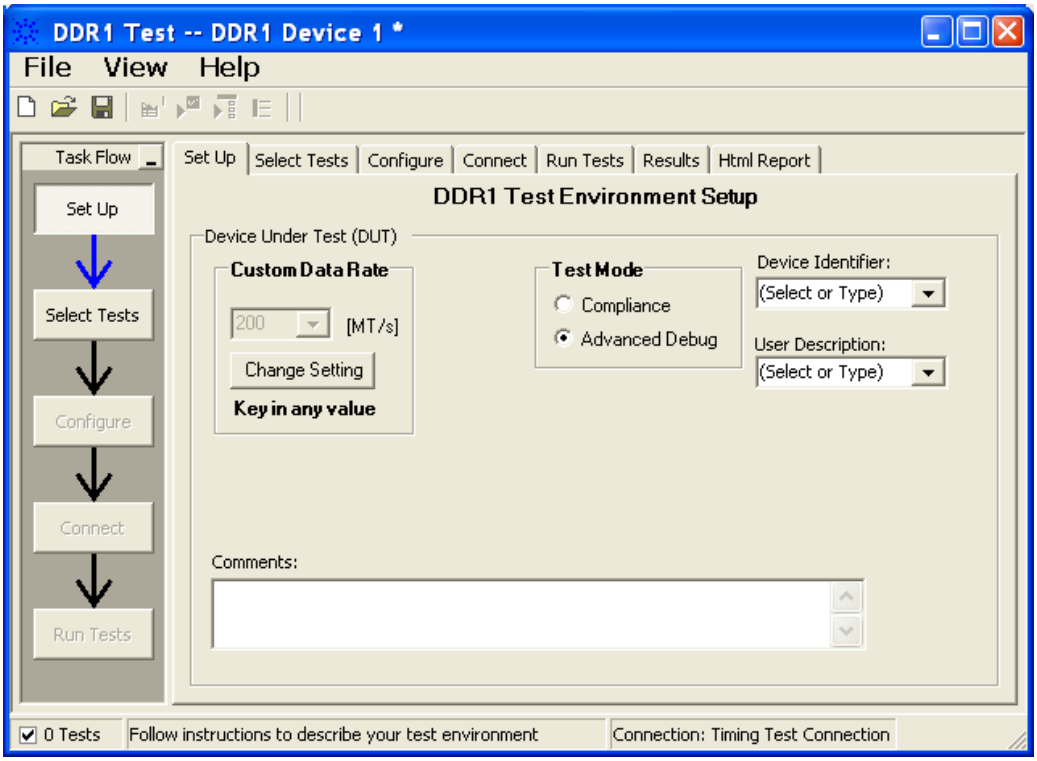


**Figure 46** Selecting Advanced Debug Mode

7 Advanced Debug also allows you to type in the data rate of the DUT signal.

8 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

9 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

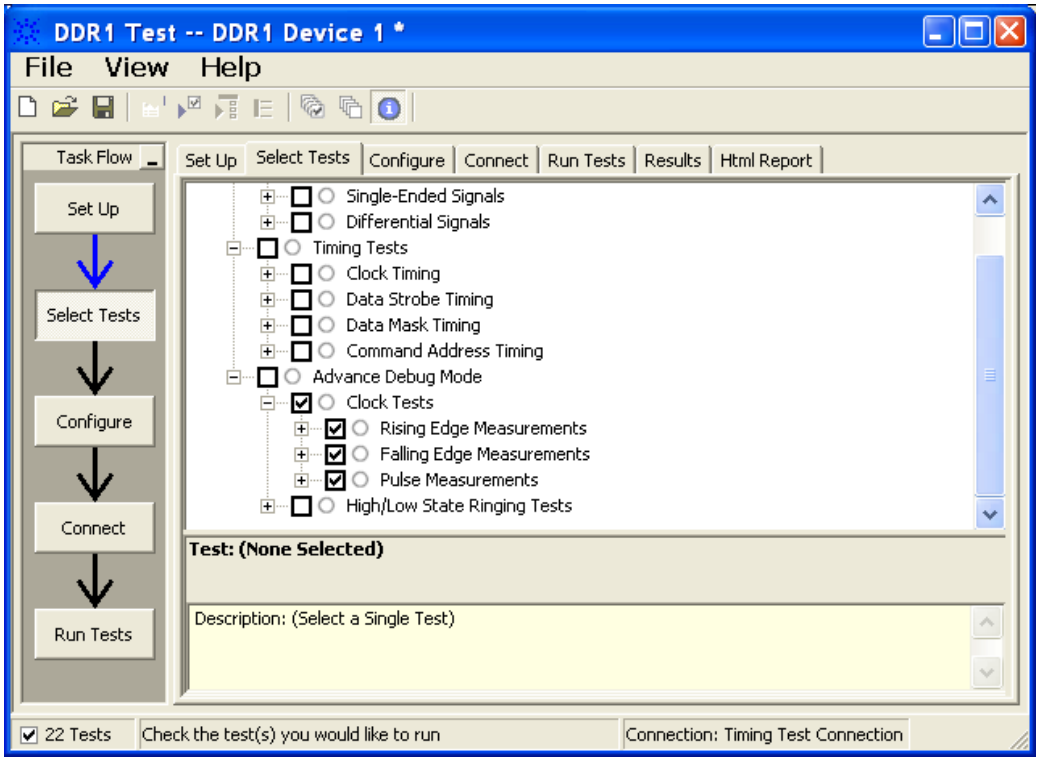


**Figure 47** Selecting Advanced Debug Clock Tests

10 Follow the DDR1 Test application's task flow to set up the configuration options (see Table 63), run the tests and view the tests results.

**Table 63** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(dc) | Input voltage high value (direct current). |
| Vih(ac) | Input voltage high value (alternating current). |
| Vil(dc) | Input voltage low value (direct current). |
| Vil(ac) | Input voltage low value (alternating current). |
| Waveform Source | Identifies the source of the data to be analyzed. |
| Use Recommended Memory Depth | Sets the Memory Depth to the maximum recommended value: 2 Mpts (DSO80000 series) or 1 Mpts (DSO548xx series). Select "No" if you plan to manually select the memory depth. |
| Use Fixed Sampling Rate and Bandwidth | Sets the Sampling Rate to 20 GSa and Bandwidth to AUTO. Select "No" if you plan to manually select sampling rate or bandwidth settings. |
| **Worst Case Tracking** | |
| Mark Worst Case Cycle | Places markers around the worst case cycles (test-dependent). Slows runtime performance. |
| **terr(nper) SubWindow Range** | |
| terr(nper) Minimum N Width Value | Sets the lower bound (inclusive) of the inner sliding window for the terr(nper) series. |
| terr(nper) Maximum N Width Value | Sets the upper bound (inclusive) of the inner sliding window for the terr(nper) series. |

# Clock Period Jitter - tJIT(per) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement and Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. You can specify the rising and/or the falling edge of your signal for this measurement.

## Signals of Interest

Based on the test definition (Read cycle only):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

## Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.
2. Compare periods with the new average.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

# Cycle to Cycle Period Jitter - tJIT(cc) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as Falling Edge Measurement. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge. The tJIT(cc) Falling Edge Measurement measures the clock period from the falling edge to falling edge. The test will show a fail status if the total failed waveforms is greater than 0.

## Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

## Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the difference between every adjacent pair of periods.
2. Generate 201 measurement results.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

# Cumulative Error - tERR(n per) - Test Method of Implementation

This Cumulative Error (across “n” cycles) test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

## Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user’s speed grade selection

## Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. tERR(2per) is similar to tJIT(per), except it makes a small 2-cycle window inside the big 200 cycle window and compares the average of the small window with the average of the big window.
2. Check the results for the smallest and largest values (worst case values).
3. Compare the results against the compliance test limits.
4. tERR(3per) is the same as tERR(2per) except the small window size is 3 periods wide. tERR(4per) uses small window size of 4 periods and tERR(5per) uses 5 periods.
5. tERR(6-10per) executes tERR(6per), tERR(7per), tERR(8per), tERR(9per) and tERR(10per), combines all the measurement results together into one big pool and checks for the smallest and largest value.
6. tERR(11-50per) does the same for tERR(11per) through tERR(50per).

# Half Period Jitter - tJIT(duty) - Test Method of Implementation

The Half Period Jitter tJIT(duty) can be divided into tJIT(CH) Jitter Average High and tJIT(LH) Jitter Average Low. The tJIT(CH) Jitter Average High Measurement measures between a positive pulse width of a cycle in the waveform, and the average positive pulse width of all cycles in a 200 consecutive cycle window. tJIT(LH) Jitter Average Low Measurement measures between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

## Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

## Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

tJIT(CH)

1. This measurement measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.
2. Measure the difference between high pulse width, and the average. Save the answer as the measurement result.
3. Compare the high pulse width with the new average.
4. Check the results for the smallest and largest values (worst case values).
5. Compare the test results against the compliance test limits.

tJIT(CH)

1. This measurement is similar to tJIT(CH) above except, instead of using high pulse widths, it uses low pulse widths for testing comparison.

# 12 Advanced Debug Mode High-Low State Ringing Tests



This section provides the Methods of Implementation (MOIs) for Advanced Debug Mode High-Low State Ringing tests using an Agilent 54850A, 80000 or 8000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR1 Compliance Test Application.

# Probing for Advanced Debug Mode High-Low State Ringing Tests

When performing the intra-pair skew tests, the DDR1 Compliance Test Application will prompt you to make the proper connections as shown in Figure 48.

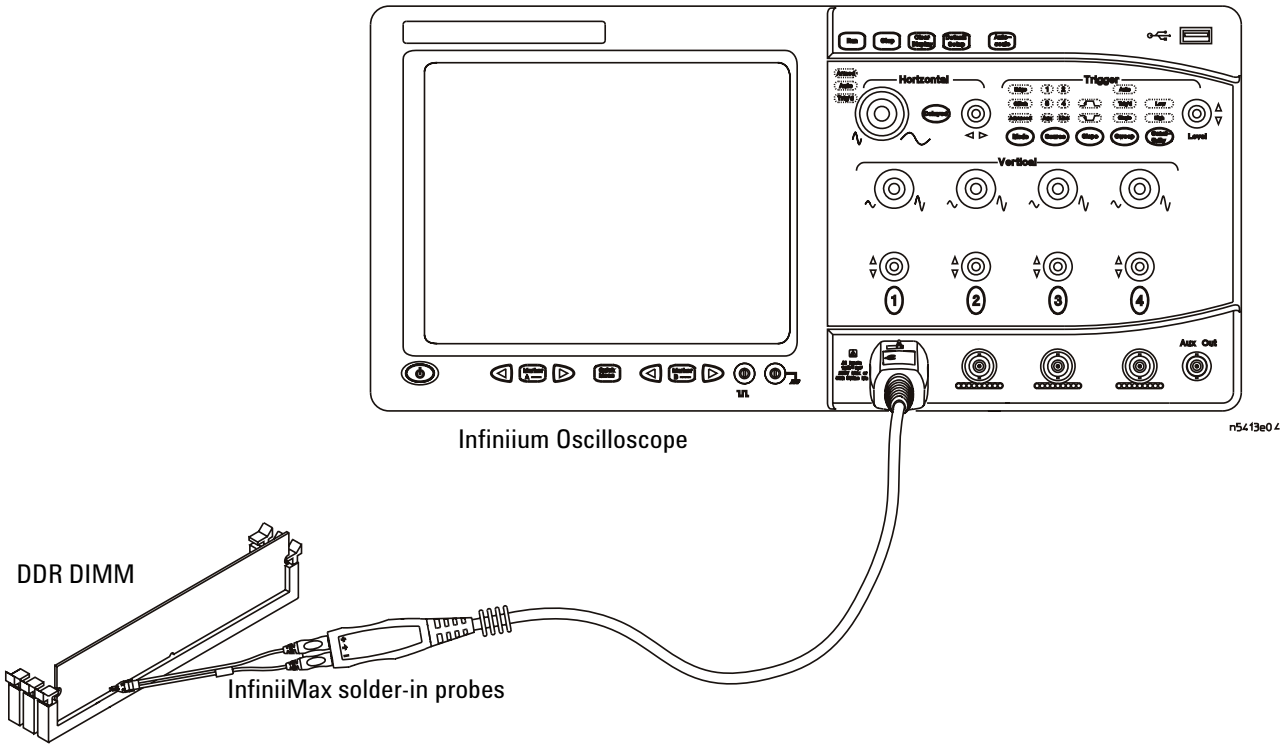


**Figure 48** Probing for Advanced Debug Mode High-Low State Ringing Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You identify the channels used for each signal in the Configuration tab of the DDR1 Compliance Test Application. (The channel shown in Figure 48 is just an example.)

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 219.

## Test Procedure

1 Start the automated test application as described in "Starting the DDR1 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR Device Under Test (DUT) is attached. This software will perform tests on all the unused RAM in the system by producing repetitive bursts of read-write data signals to the DDR memory.

3 Connect the differential solder-in probe head to the PUT on the DDR DIMM.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR1 test application, click the Set Up tab.

6 Select Advanced Debug as the Test Mode option.

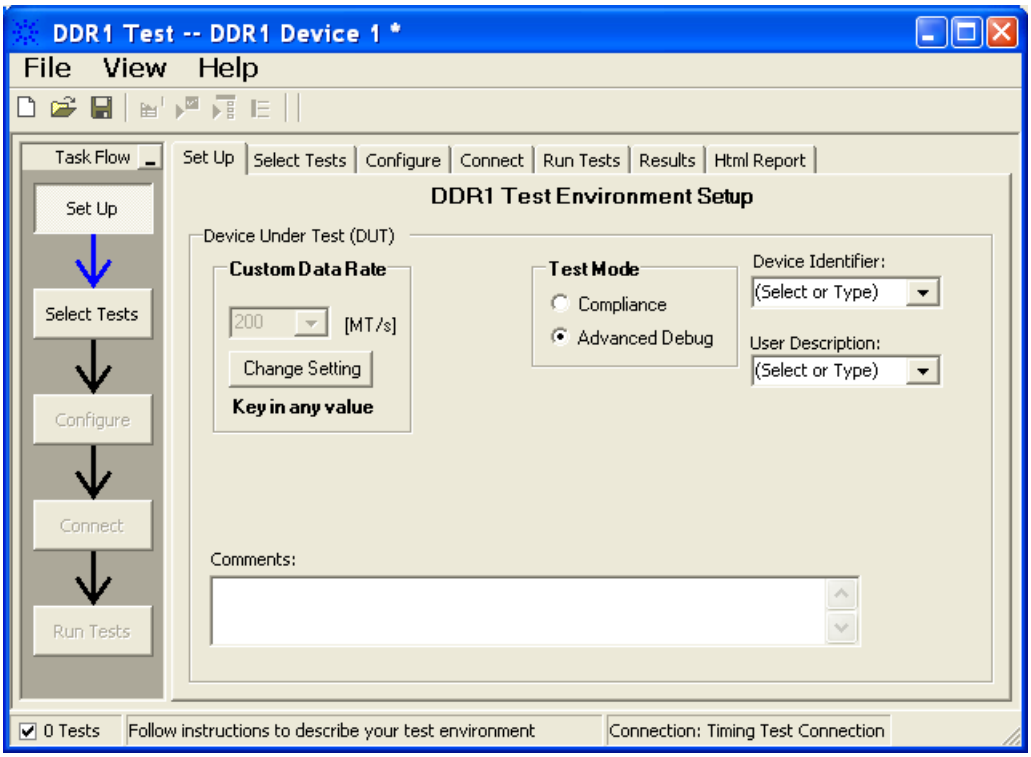


**Figure 49** Selecting Advanced Debug Mode

7 Advanced Debug also allows you to type in the data rate of the DUT signal.

8 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

9 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

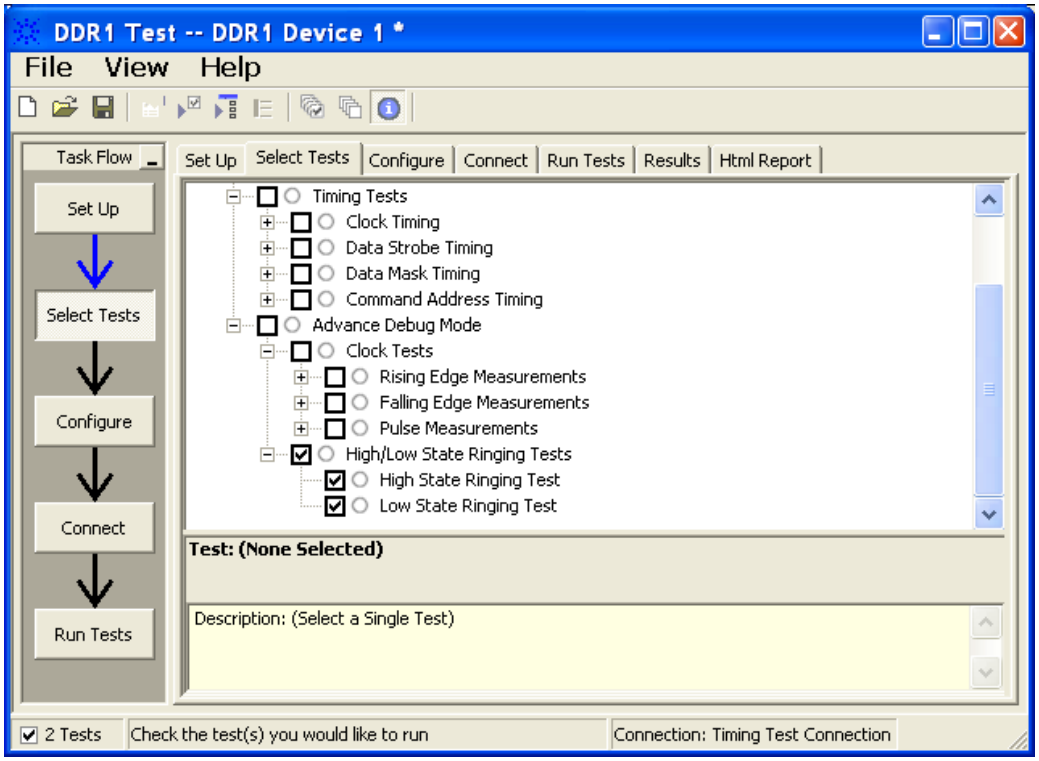


**Figure 50** Selecting Advanced Debug High-Low State Ringing Tests

10 Follow the DDR1 Test application's task flow to set up the configuration options (see Table 64), run the tests and view the tests results.

**Table 64** Test Configuration Options

| Configuration Option | Description |
|---|---|
| Stop on error | Enabling this error message will allow error message to prompt whenever criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and continue to the next test. This option is suitable for long hours multiple trial. |
| Signal Threshold setting by percentage | This option allow user to define the Upper and Lower threshold of the signal by percentage. |
| VDD | Input supply voltage value. |
| VDDQ | Input supply voltage for data output. |
| Vref | Input reference voltage value. |
| Vih(DC) | Input voltage high value (direct current). |
| Vih(AC) | Input voltage high value (alternating current). |
| Vil(DC) | Input voltage low value (direct current). |
| Vil(AC) | Input voltage low value (alternating current). |
| **Advanced Debug Mode** | |
| Pin Under Test, PUT | Identifies the Pin Under Test for High/Low State Ringing tests |
| PUT Source | Identifies the source of the PUT for High-Low State Ringing tests. |
| Time-out | Identifies the time-out value to be used for High-Low State Ringing Test. |
| Trigger Level | Sets the rising edge voltage level to trigger on for all High-Low State Ringing Test. |
| Upper Level | Identifies the upper threshold level to be used for the ringing tests. |
| Hysteresis | Identifies the hysteresis value to be used for the ringing test. |
| Lower Level | Identifies the lower threshold level to be used for the ringing tests. |

## High State Ringing Tests Method of Implementation

The Advanced Debug Mode Ringing test can be divided into two sub-tests. One of them is the High State Ringing test. There is no available specification for this test in the *JEDEC Standard JESD79E* specifications. The ringing debug test is definable by the customers to capture the glitch of interest for the logic high state section in a test signal for evaluation purposes. The purpose of this test is to automate all the required setup procedures, particularly the InfiniiScan RUNT mode setup, to capture the ringing section of a test signal. Users are required to customize the threshold value in the Configure tab to capture the specific RUNT signals. The expected results are signals captured on the screen that fulfill the InfiniiScan RUNT criteria. There is a pulse in the captured signal that passes through two voltage level threshold but not the third.

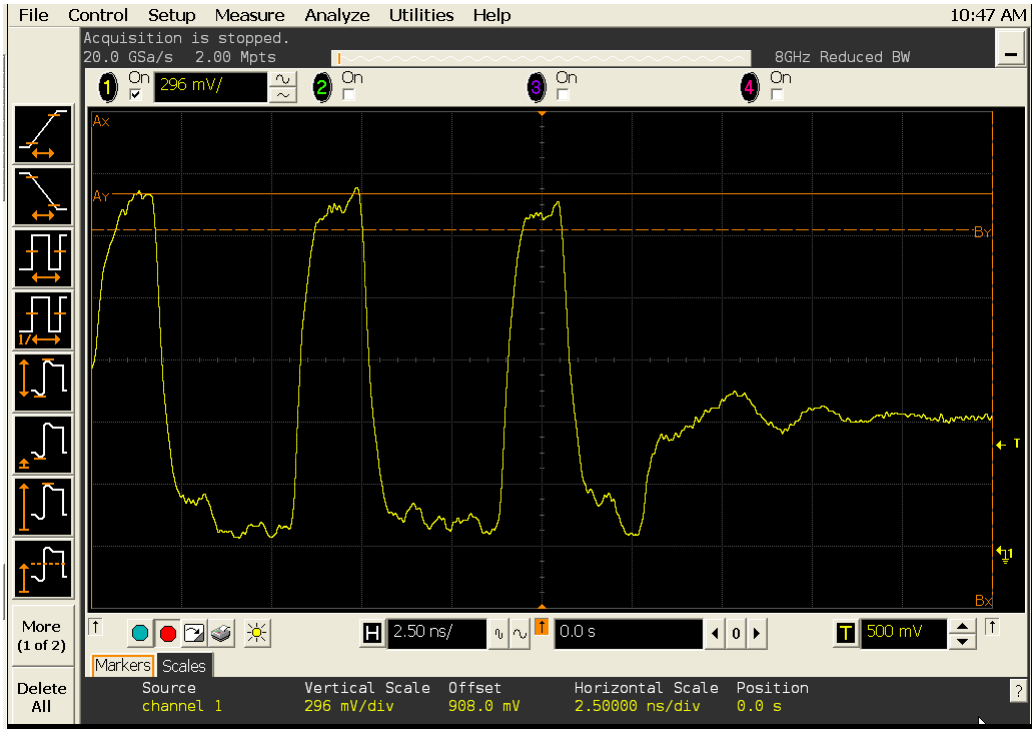


**Figure 51** High State Ringing Test

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signals OR
- Data Strobe Signals OR
- Address Signals OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against the user's speed grade selection

## Measurement Algorithm

1. Acquire initial signal data and then perform signal conditioning to maximize the screen resolution - vertical scale adjustment.
2. Setup the InfiniiScan to activate the RUNT mode.
3. Acquire test data with the InfiniiScan RUNT activated.
4. Display Markers to show the RUNT Upper Level and RUNT Lower Level.

## Low State Ringing Tests Method of Implementation

Just as the High State Ringing test, there is no available specification in the *JEDEC Standard JESD79E* specifications for the Low State Ringing tests. The ringing debug test is definable by the customers to capture the glitch of interest for the logic low state section in a test signal for evaluation purposes. The purpose of this test is to automate all the required setup procedures, particularly the InfiniiScan RUNT mode setup, to capture the ringing section of a test signal. Users are required to customize the threshold value in the Configure tab to capture the specific RUNT signals. The expected results are signals captured on the screen that fulfill the InfiniiScan RUNT criteria. There is a pulse in the captured signal that passes through two voltage level threshold but not the third.

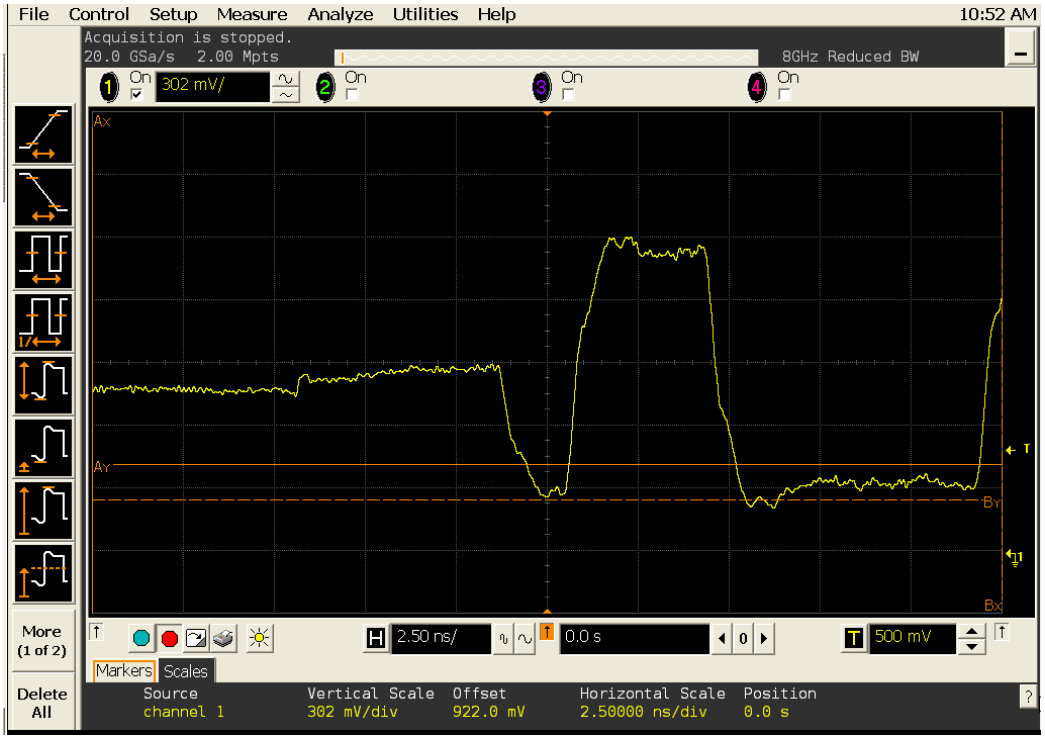


**Figure 52** Low State Ringing Test

## Signals of Interest

Based on the test definition (Write cycle only):

- Data Signals OR
- Data Strobe Signals OR
- Address Signals OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

## Measurement Algorithm

1. Acquire initial signal data and then perform signal conditioning to maximize the screen resolution - vertical scale adjustment.
2. Setup the InfiniiScan to activate the RUNT mode.
3. Acquire test data with the InfiniiScan RUNT activated.
4. Display Markers to show the RUNT Upper Level and RUNT Lower Level.

# 13 Calibrating the Infiniium Oscilloscope and Probe



This section describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

## Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DDR1 automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the 54850A, 8000 and 80000 series Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.
- BNC shorting cap (provided with the 54850A series Infiniium oscilloscopes).

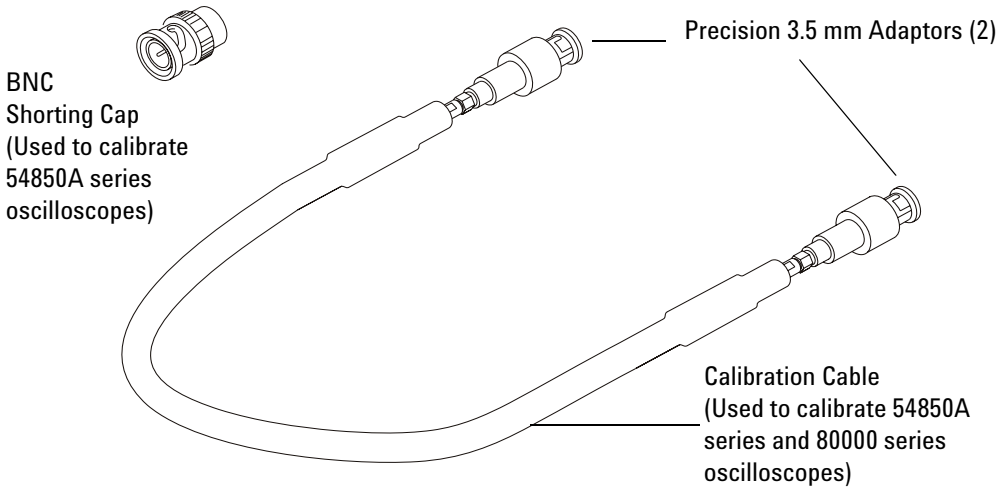


**Figure 53** Accessories Provided with the Agilent Infiniium Oscilloscope

## Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   **a** Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   **b** Plug in the power cord.

   **c** Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   **d** Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 54 below, perform the following steps:

   a Click on the Utilities>Calibration menu to open the Calibration dialog box.

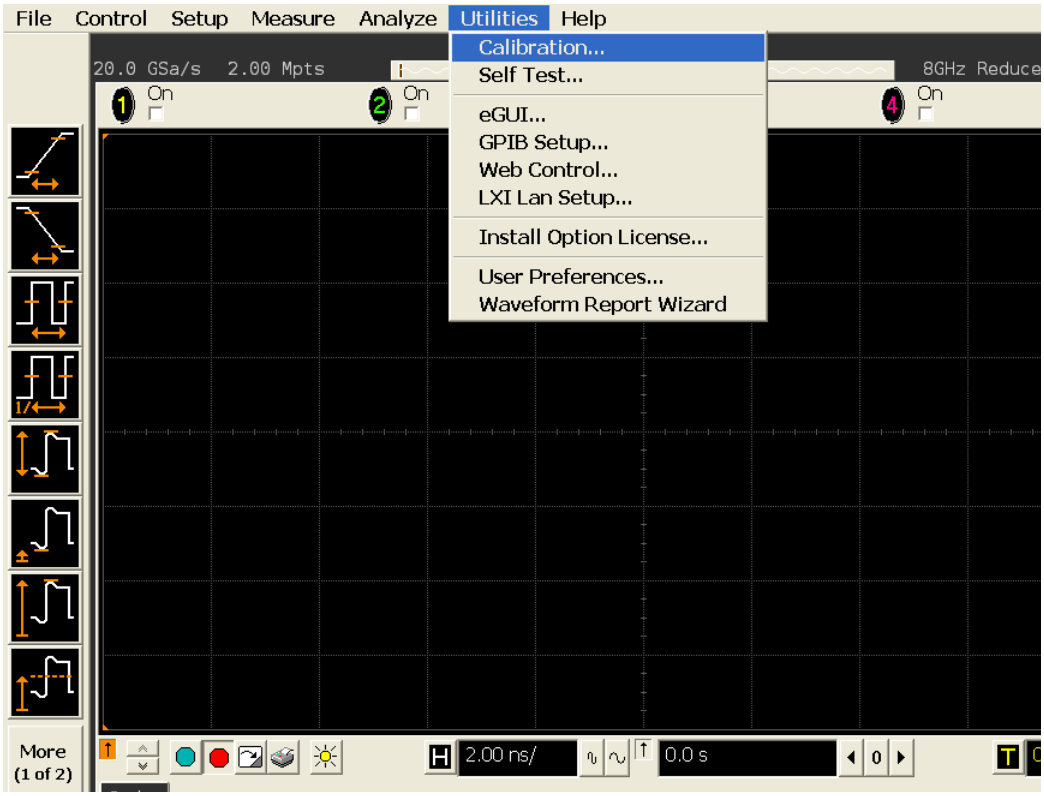


**Figure 54** Accessing the Calibration Menu

4 Referring to Figure 55 below, perform the following steps to start the calibration:

   b Uncheck the Cal Memory Protect checkbox.

   c Click the Start button to begin the calibration.

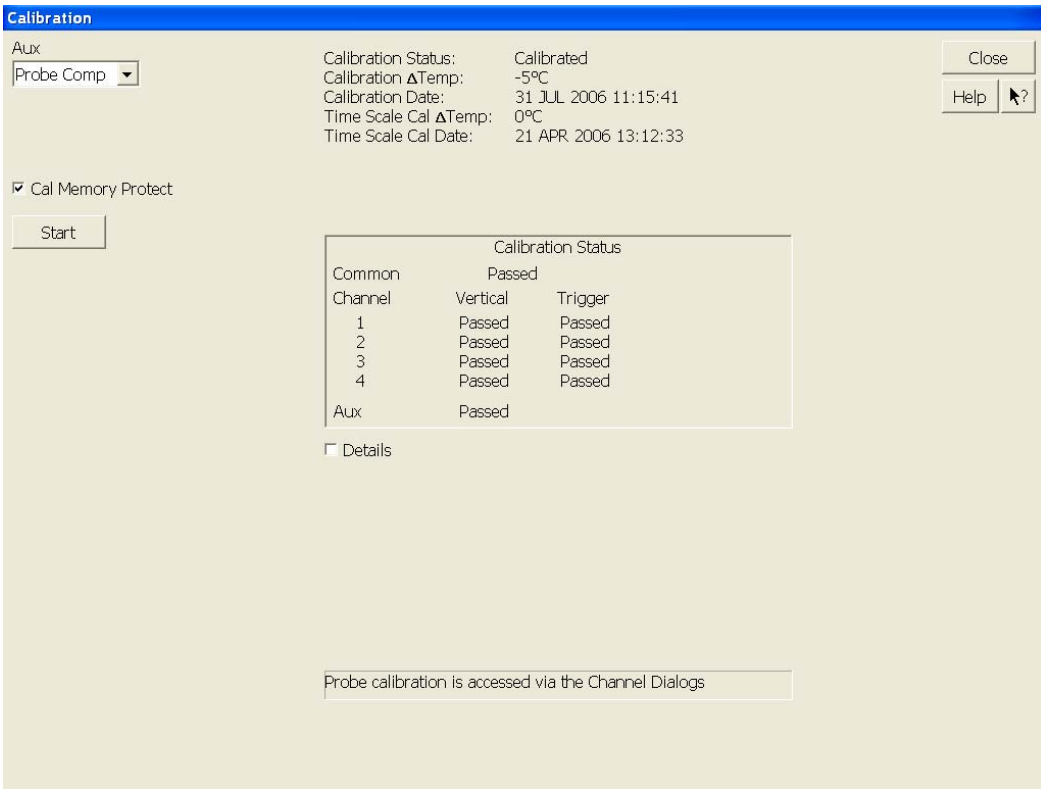


**Figure 55** Oscilloscope Calibration Window

**d** During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 56 below.

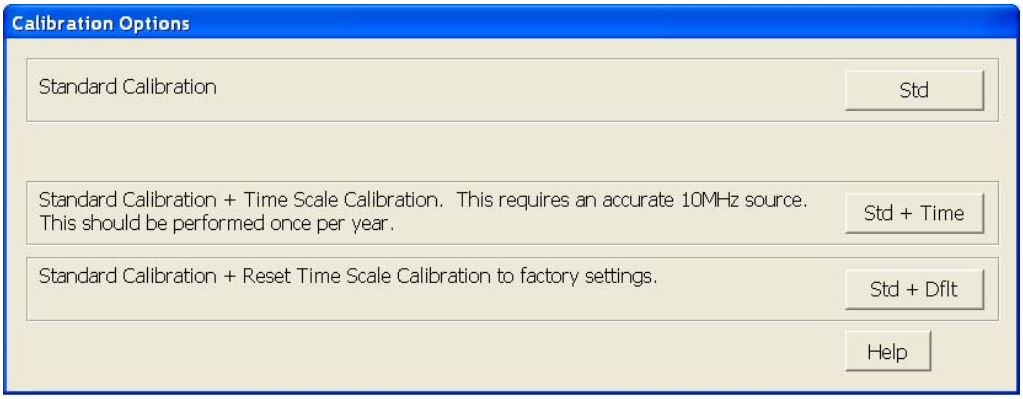


**Figure 56** Time Scale Calibration Dialog box

e Click on the Std+Dflt button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

g Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

h Click the Close button to close the calibration window.

i The internal calibration is completed.

j Read NOTE below.

**NOTE** These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

## Required Equipment for Probe Calibration

Before performing DDR1 tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

# Probe Calibration

## Connecting the Probe for Calibration

For the following procedure, refer to Figure 57 below.

1. Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.
3. Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
4. Connect the probe to an oscilloscope channel.
5. To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
6. Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
7. Release the yellow pincher.

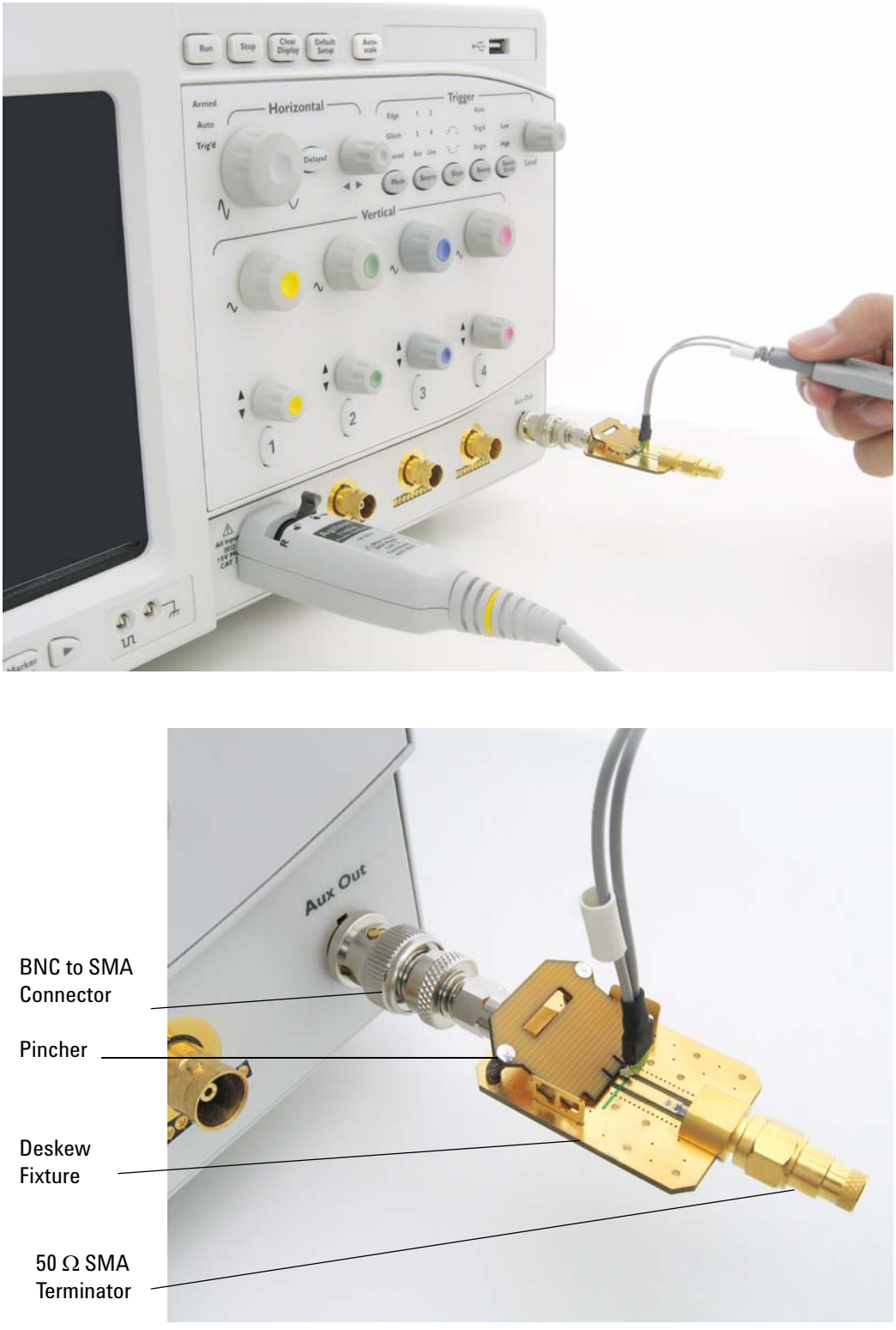


**Figure 57** Solder-in Probe Head Calibration Connection Example

## Verifying the Connection

1 On the Infiniium oscilloscope, press the autoscale button on the front panel.

2 Set the volts per division to 100 mV/div.

3 Set the horizontal scale to 1.00 ns/div.

4 Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 58 below.

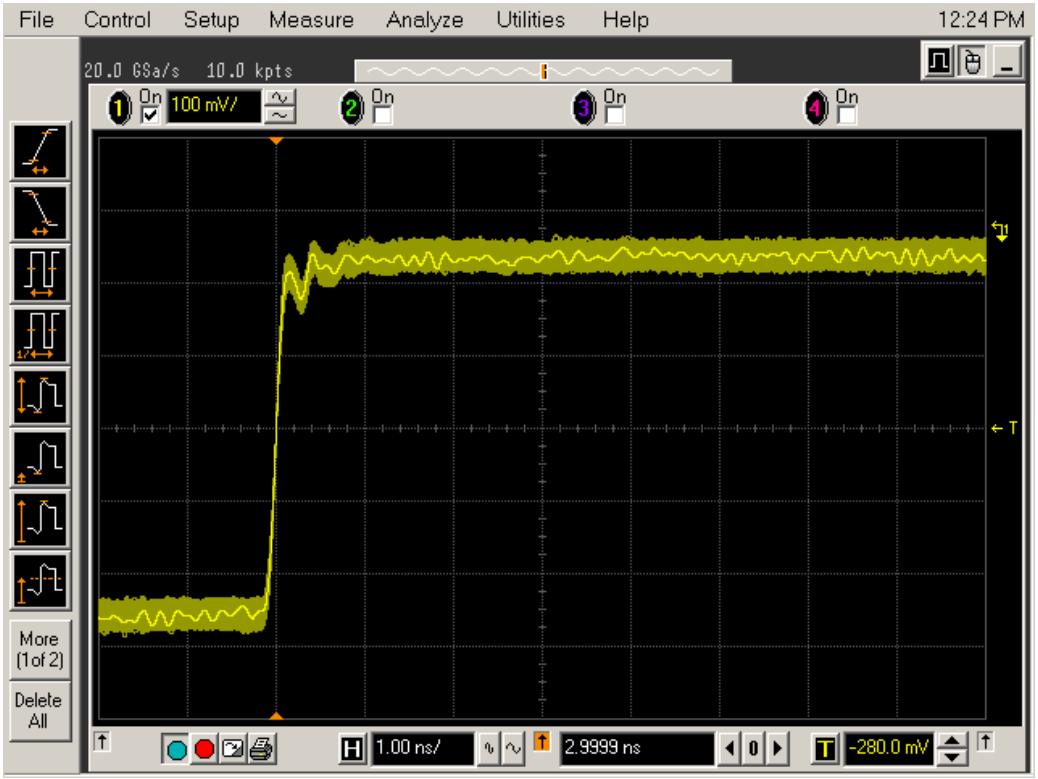


**Figure 58** Good Connection Waveform Example

If you see a waveform similar to that of Figure 59 below, then you have a bad connection and should check all of your probe connections.

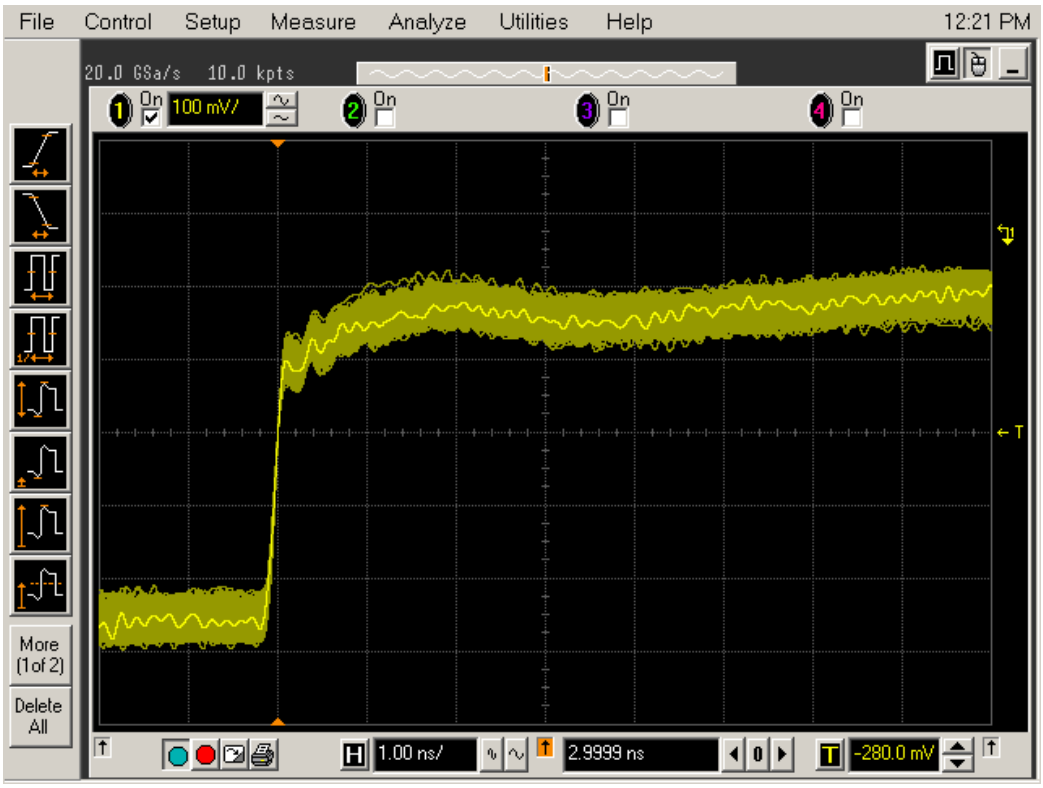


**Figure 59** Bad Connection Waveform Example

## Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 60.

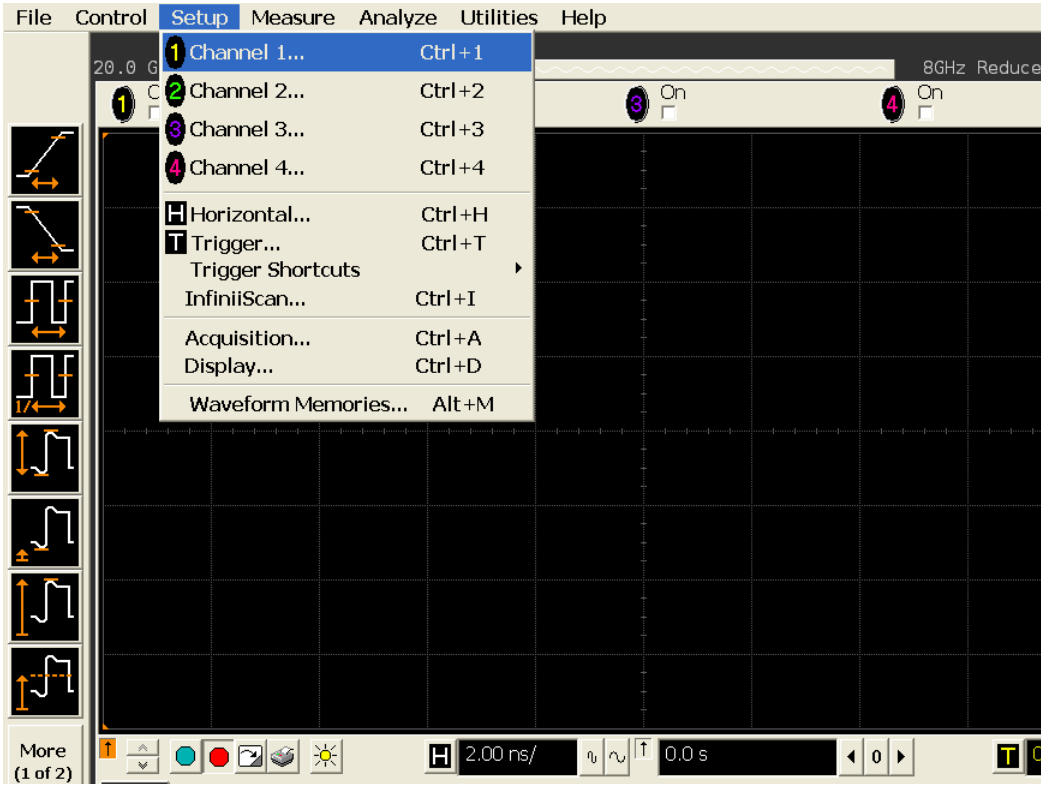


**Figure 60** Channel Setup Window.

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 61.

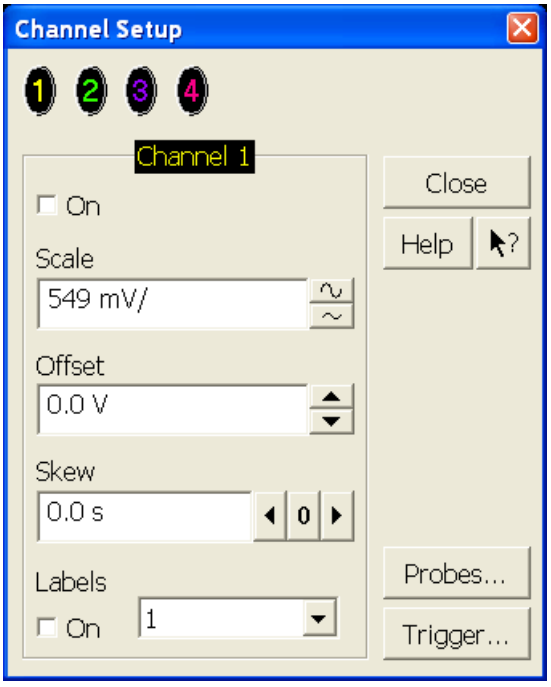


**Figure 61** Channel Dialog Box

**3** In the Probe Setup dialog box, select the Calibrate Probe... button.

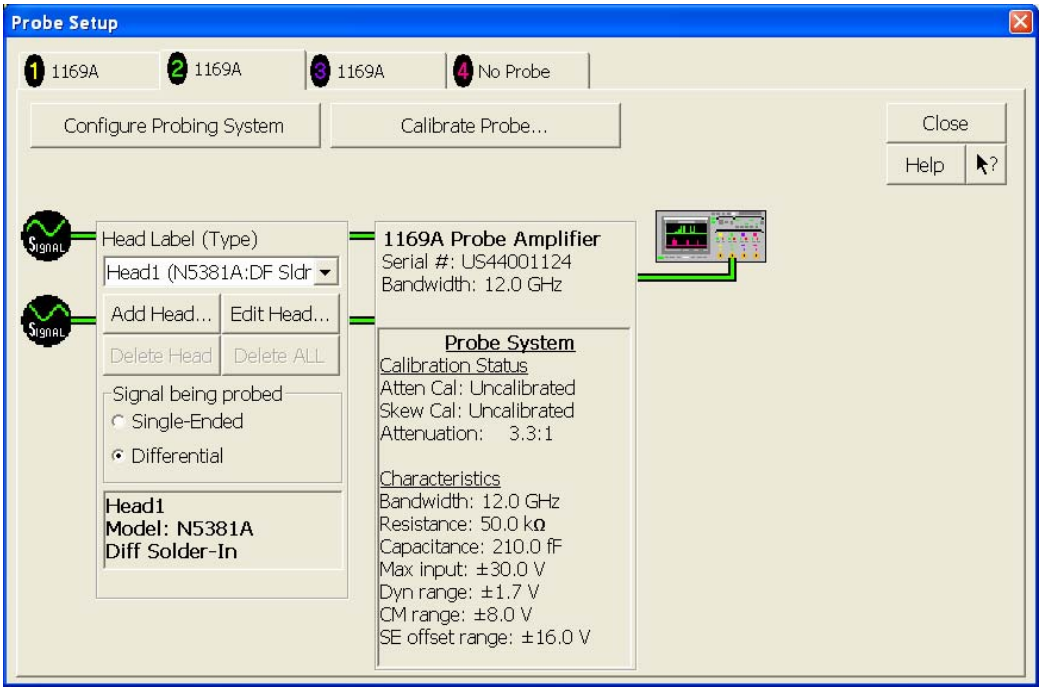


**Figure 62** Probe Setup Window.

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

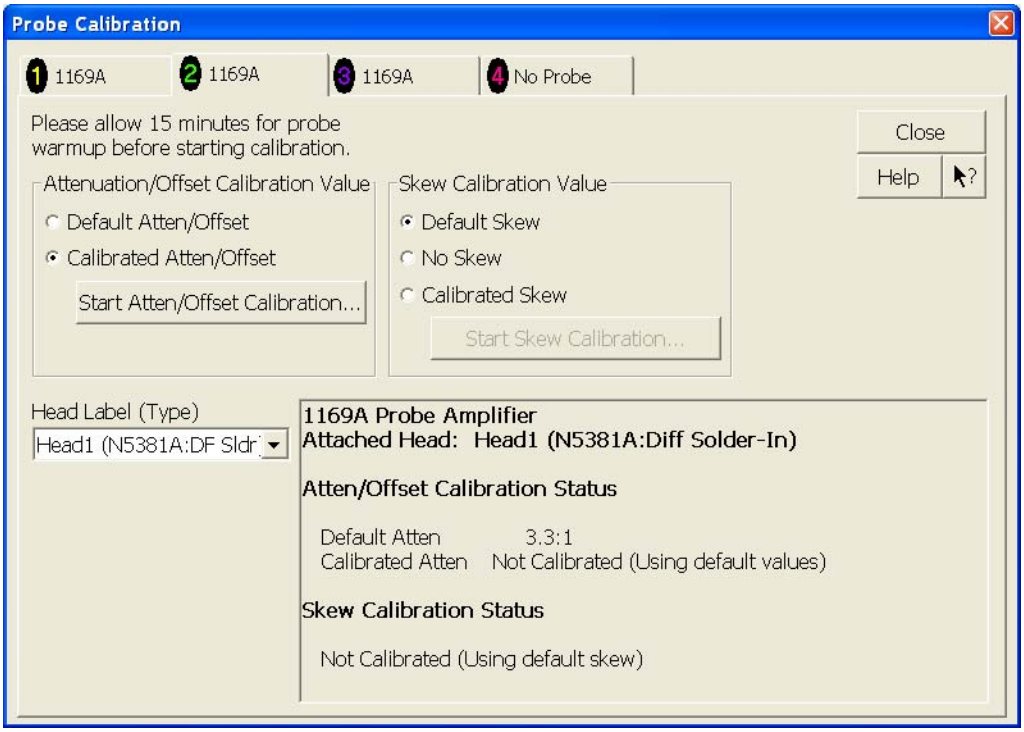


**Figure 63** Probe Calibration Window.

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

## Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adaptor
- SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Agilent 8120-1838
- Agilent 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Agilent 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 64.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.

3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.

4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

5 Connect the probe to an oscilloscope channel.

6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

8 Release the yellow pincher.

9 On the oscilloscope, press the autoscale button on the front panel.

10 Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.

11 Select the Probes... button.

12 Select the Configure Probe System button.

13 Select User Defined Probe from the pull-down menu.

14 Select the Calibrate Probe... button.

15 Select the Calibrated Skew radio button.

16 Once the skew calibration is completed, close all dialog boxes.

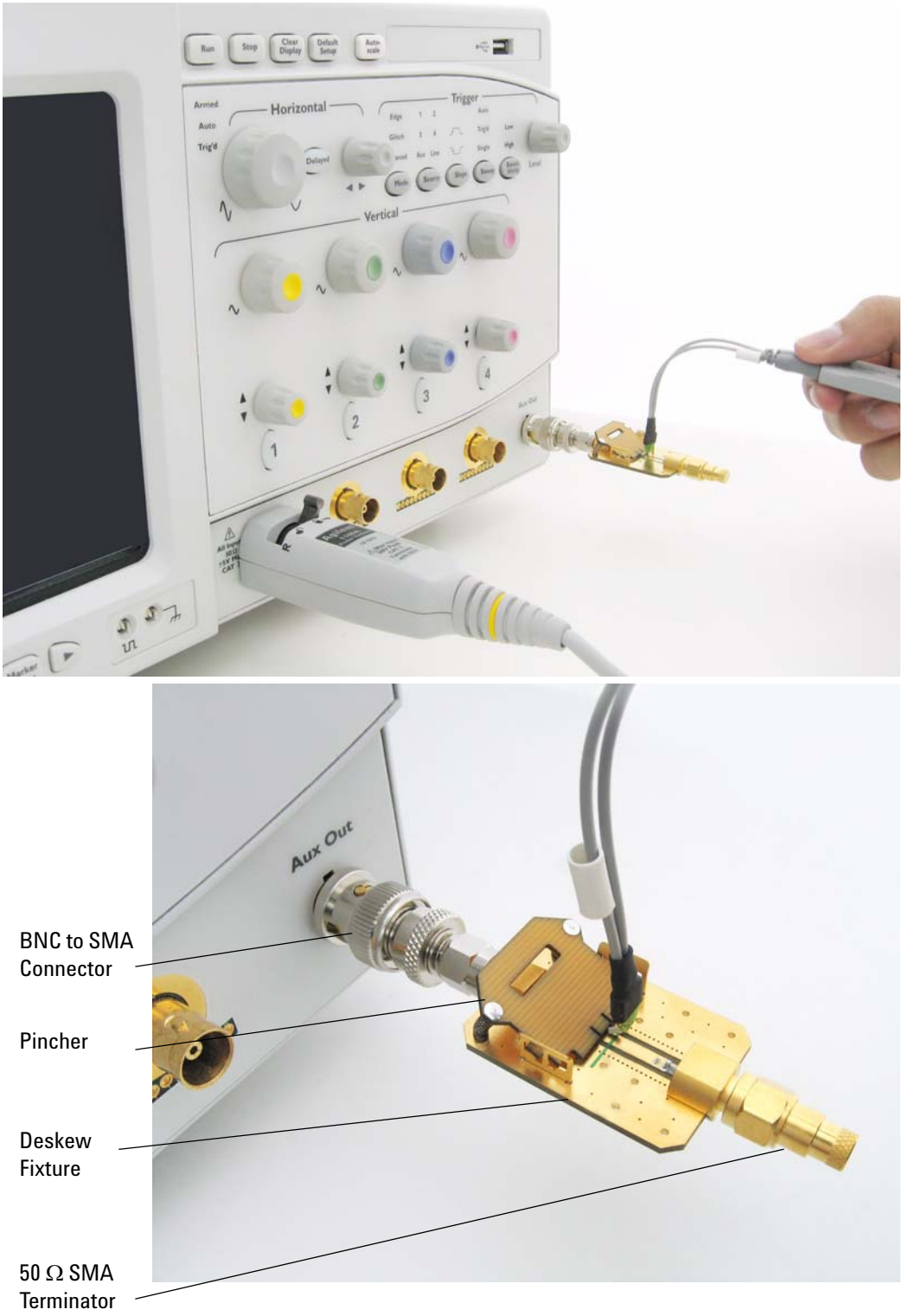


**Figure 64** Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.

18 Set the vertical scale for the displayed channels to 100 mV/div.

19 Set the horizontal range to 1.00 ns/div.

20 Set the horizontal position to approximately 3 ns.

21 Change the vertical position knobs of both channels until the waveforms overlap each other.

22 Select the Setup menu choose Acquisition... from the pull-down menu.

23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 65.

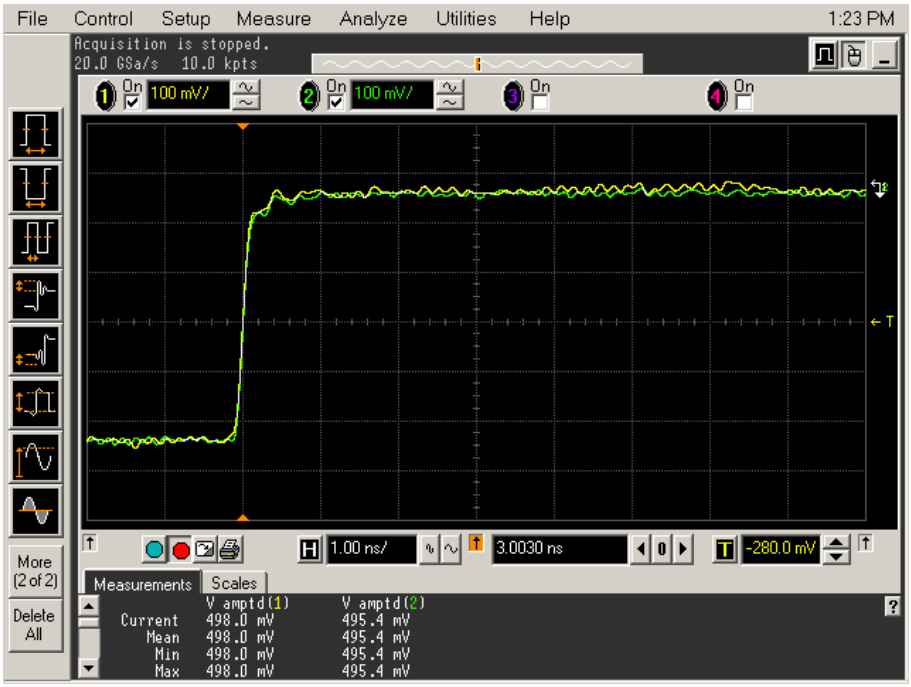


**Figure 65** Calibration Probe Waveform Example

**NOTE**

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

# 14 InfiniiMax Probing


**Figure 66** 1134A InfiniiMax Probe Amplifier

Agilent recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz.

Agilent also recommends the E2677A differential solder-in probe head. Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5382A InfiniiMax II 12 GHz differential browser, E2675A InfiniiMax differential browser probe head, N5425A InfiniiMax ZIF probe head and N5426A ZIF Tips.

**Figure 67** E2677A / N5381A Differential Solder-in Probe Head

**Table 65** Probe Head Characteristics (with 1134A probe amplifier)

| Probe Head | Model Number | Differential Measurement (BW, input C, input R) | Single-Ended Measurement (BW, input C, input R) |
|---|---|---|---|
| Differential Solder-in | E2677A | 7 GHz, 0.27 pF, 50 kOhm | 7 GHz, 0.44 pF, 25 kOhm |

Used with 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidth respectively.

# 15 Common Error Messages



When performing DDR1 tests, error message dialog boxes can occur due to improper configuration settings. This section describes the common errors, causes and solution to the problem.

## Required Triggering Condition Not Met

The following error message will appear when a time-out occurs. This error message indicates that the required triggering condition is not met. This is followed by test cancellation and aborting message. All pending tests will be cancelled.

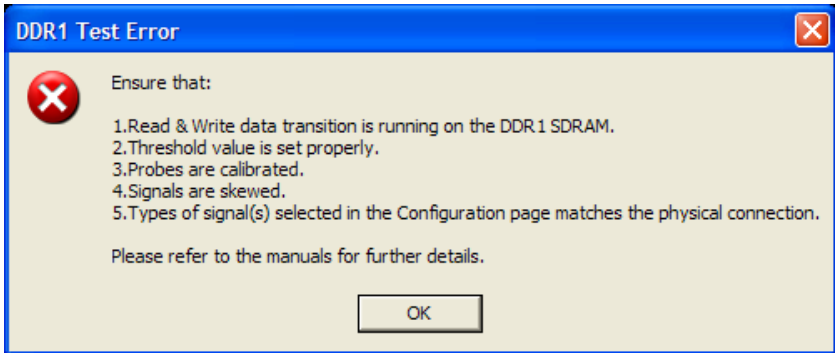


**Figure 68** Required Trigger Condition Not Met Error Message

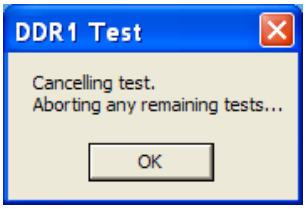


**Figure 69** Cancel and Abort Test Message

These error dialog boxes appear when one of the following configuration errors is encountered.

- Required triggering condition is not met. For example, if the setup time condition in a triggering requirement, is not met within a certain time (approximately 10s), the time-out error will occur.
- Attempt to run the Electrical tests without first executing the RAM reliability test software on the DDR Device Under Test (DUT) system.
- Attempt to run the Electrical tests without providing any test signal to the oscilloscope.
- Threshold value is not properly set.
- Signals are not skewed.
- The type of signals selected in the Configuration page does not match the physical connection.

Ensure that:

- The RAM reliability test software is running to exercise the SDRAM. This ensures that there are Read and Write signals running on the SDRAM in order for the application to capture the signal.
- The threshold is properly set according to the actual signal performance. For example, if the maximum voltage of the DQ signal is 1.8V and the minimum voltage is 40mV, you must ensure that the upper and lower threshold value does not exceed the minimum and maximum limit, in order to trigger the signal. Scope will not be triggered if the upper threshold is set to be above 1.8V, since the maximum voltage on the actual signal is just 1.8V and below.
- The probes are properly calibrated and skewed. Ensure that correct probes are used and they are properly calibrated, so that it reflects the actual signal and is not over or under amplified. Similarly, ensure that the channels are properly soldered on the DDR1 module and ensure that the signals are not over skewed.
- The types of signals selected in the Configuration page matches the physical connection. For example, if Channel 1 is physically connected to the Clock signal, ensure that you select the same in the Configuration page.

## Software License Error

When you load the N5413A DDR1 Compliance Test Application, it checks for the required software licenses. When one of the optional licenses is not detected, the application will limit the available test options and the Set Up tab will look similar to following screenshot.

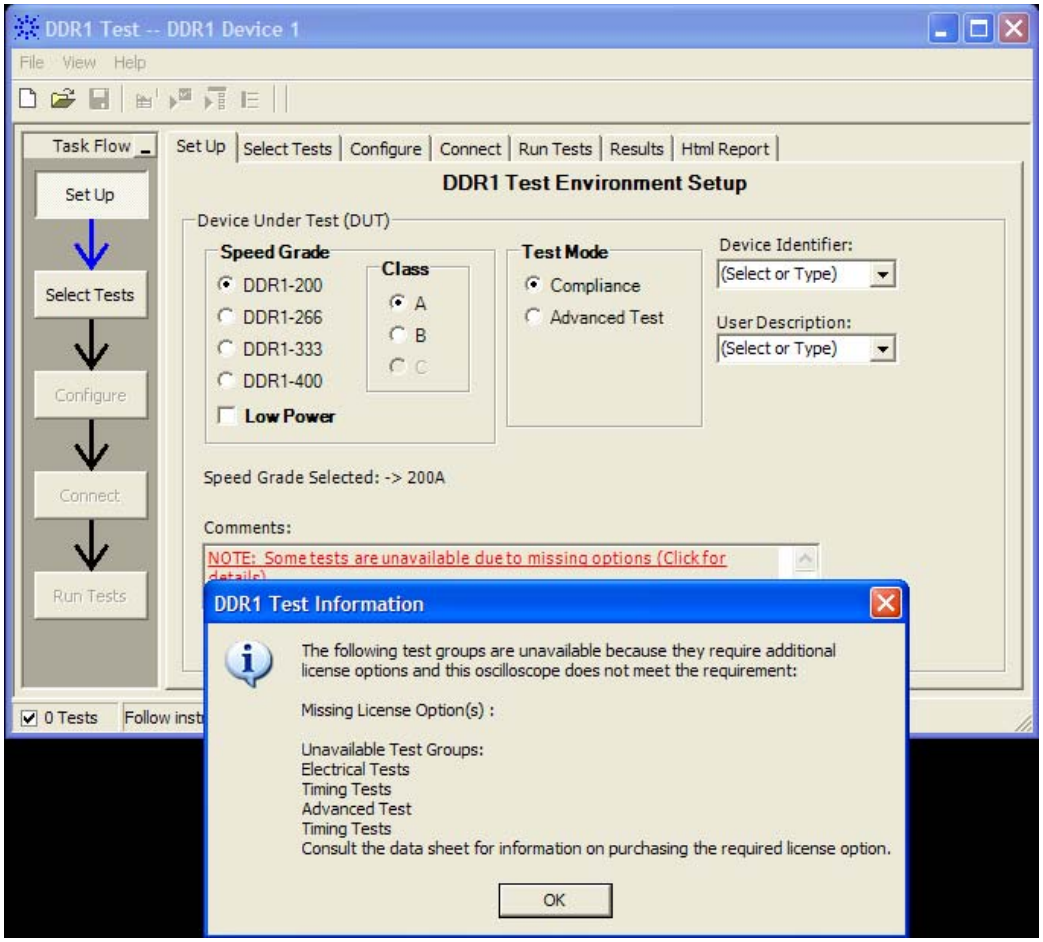


**Figure 70** Software License Error

Ensure you have installed all required licenses before running the N5413A DDR1 Compliance Test Application.

## Frequency Out of Range Error

You are allowed to type in the DUT data rate for the Advanced Debug Mode tests. However, if you enter an incorrect data strobe test signal frequency, the following error dialog box appears. For example, if the selected DDR1 speed grade option is DDR1-400, the expected frequency of the data strobe signal, DQS is 200MH (half of the data transfer rate). However, if the measured DQS frequency is out by +/-10% of the expected frequency value, exception will be thrown.

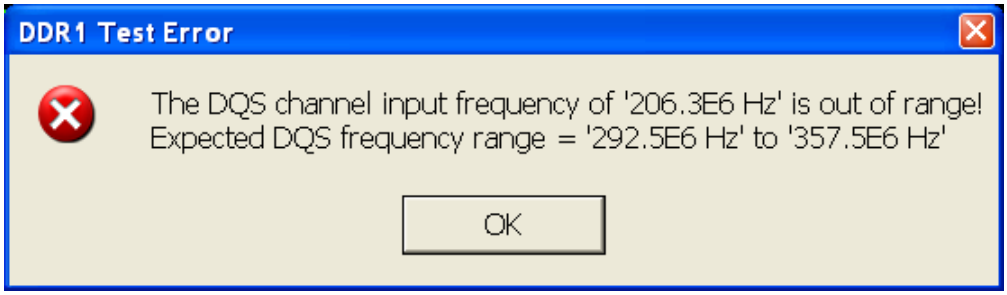


**Figure 71** Frequency Out of Range Error

Type in the correct data rate, within the range, as mentioned in the error message box.

## Missing Signal Error

This error occurs when the required signals are either not selected in the “Channel Setting” configuration or not connected to the oscilloscope. Ensure that correct channel is selected based on the signal that is physically present at the oscilloscope channel.


**Figure 72** Missing Signal Error Message

## Invalid Pre/PostAmble Signal Error

This error occurs during the multiple trial run if there is no significant voltage level transits when the driver is turned on or off during the preamble or postamble. You should verify the signals especially the DQS and DQ if they provide a valid preamble or postamble signal. If there is no significant voltage level transition when the driver is turned on or off during the pre-amble OR post-amble, the system will throw an exception to prompt user to verify the signal.

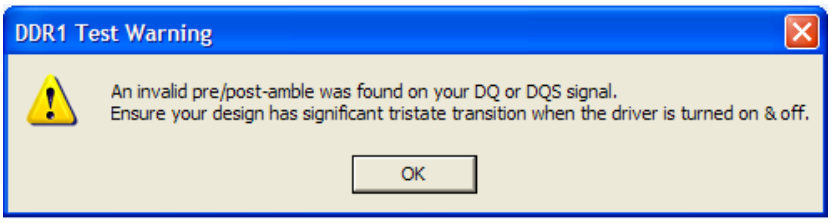


**Figure 73** Invalid Pre/Post Amble Signal Error Message

You can disable this error message at the Configure tab. Turn the “Signal error message prompt” to the Disable mode. This will prevent the above error message being prompt during the multiple trial run.

# Index

## V



## W



## Z

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